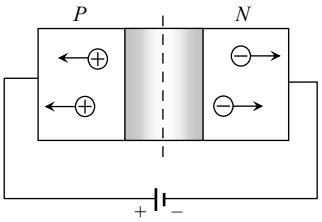
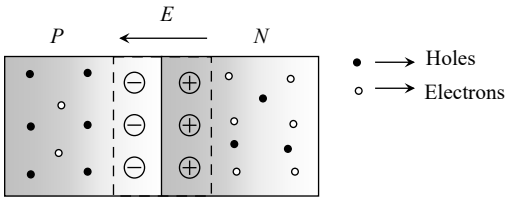
Semiconductor Diode

1. (b)
2. (a) In forward biased *PN*-junction, external voltage decreases the potential barrier, so current is maximum. While in reversed biased *PN*-junction, external voltage increases the potential barrier, so the current is very small.
3. (b)
4. (b) Filter circuits are used to get smooth *dc* π-filter is the best filter.
5. (c) In reverse bias no current flows.
6. (b) In reverse biasing, width of depletion layer increases.
7. (a) Depletion layer consist of mainly stationary ions.
8. (b) Current flow is possible and $i = \frac{V}{R} = \frac{(4-1)}{300} = 10^{-2}\,A$
9. (a) The potential of *P*-side is more negative that of *N*-side, hence diode is in reverse biasing. In reverse biasing it acts as open circuit, hence no current flows.
10. (a)
11. (b) It is used to convert *ac* into *dc* (rectifier)



12. (b)
13. (b) Because in case (1) N is connected with N. This is not a series combination of transistor.
14. (c)
15. (d)
16. (c) After a large reverse voltage is *PN*-junction diode, a huge current flows in the reverse direction suddenly. This is called Breakdown of *PN*-junction diode.
17. (c) In forward biasing both positive and negative charge carriers move towards the junction.
18. (b,c)
19. (c) When polarity of the battery is reversed, the *P*-*N* junction becomes reverse biased so no current flows.
20. (d) Resistance in forward biasing $R_{fr} \approx 10\,\Omega$ and resistance in reverse biasing $R_{Rw} \approx 10^5\,\Omega \Rightarrow \frac{R_{fr}}{R_{Rw}} = \frac{1}{10^4}$
21. (d)
22. (b) In forward biasing width of depletion layer decreases.
23. (d)
24. (c) At junction a potential barrier/depletion layer is formed, with *N*-side at higher potential and *P*-side at lower potential. Therefore there is an electric field at the junction directed from the *N*-side to *P*-side



25. (c) In *N*-type semiconductor majority charge carriers are electrons.
26. (b) In forward biasing the diffusion current increases and drift current remains constant so not current is due to the diffusion.
    In reverse biasing diffusion becomes more difficult so net current (very small) is due to the drift.
27. (b) At a particular reverse voltage in *PN*-junction, a huge current flows in reverse direction known as avalanche current.

28. (b) Due to the large concentration of electrons in *N*-side and holes in *P*-side, they diffuses from their own side to other side. Hence depletion region produces.

29. (c) Only in option (c), *P*-side is more negative as compared to *N*-side.

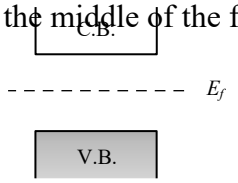
30. (b) Depletion layer is more in less doped side.

31. (b) In forward biasing *P*-side is connected with positive terminal and *N*-side with negative terminal of the battery

32. (c) In forward biasing of *PN*-junction diode, current mainly flows due to the diffusion of majority charge carriers.

33. (d)

34. (c) In forward biasing of *PN* junction diode width of depletion layer decreases. In intrinsic semiconductor fermi energy level is exactly in the middle of the forbidden gap



35. (d)

36. (a) At high reverse voltage, the minority charge carriers, acquires very high velocities. These by collision break down the covalent bonds, generating more carriers. This mechanism is called Avalanche breakdown.

37. (b) Because *P*-side is more negative as compared to *N*-side.

38. (b) When reverse bias is increased, the electric field at the junction also increases. At some stage the electric field breaks the covalent bond, thus the large number of charge carriers are generated. This is called Zener breakdown.

39. (d) In forward biasing both V_B and x decreases.

40. (a)

41. (b) In figure 2,4 and 5. *P*-crystals are more positive as compared to *N*-crystals.

42. (a) $ac \longrightarrow$ Rectifier $\longrightarrow dc$

43. (b) In this condition $P-N$ junction is reverse biased.

44. (a)

45. (a) $E = \frac{V}{d} = \frac{0.5}{5\times10^{-7}} = 10^6 \ V/m.$

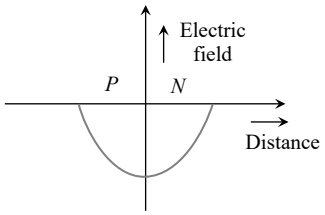
46. (b) Across the $P-N$ junction, a barrier potential is developed whose direction is from N region to P region.

47. (b)

48. (a) In forward biasing, resistance of PN junction diode is zero, so whole voltage appears across the resistance.

49. (c)

50. (d) The electric field strength versus distance curve across the *P*-*N* junction is as follows



51. (d)

52. (a) It doesn't Obey's ohms law.

53. (c) Because *N*-side is more positive as compared to *P*-side.

54. (c) When a light (wavelength sufficient to break the covalent bond) falls on the junction, new hole electron pairs are created. No. of produced electron hole pair deponed upon no. of photons. So photo emf or current proportional to intensity of light.

55. (b)

56. (d) For full wave rectifier $\eta = \frac{81.2}{1+\frac{r_f}{R_L}}$

$\Rightarrow \eta_{max} = 81.2\% \qquad (r_f << R_L)$

57. (a)

58. (a)

59. (c) In reverse biasing negative terminal of the battery is connected to *N*-side.

60. (a) In the given condition diode is in reverse biasing so it acts as open circuit. Hence potential difference between *A* and *B* is $6V$

61. (b) Zener breakdown can occur in heavily doped diodes. In lightly doped diodes the

necessary voltage is higher, and avalanche multiplication is then the chief process involved.

62. (c)

63. (a)

64. (c) Diode acts as open switch only when it is reverse biased

65. (a) Because *P*-side is more negative than *N*-side.

66. (b) In unbiased condition of *PN*-junction, depletion region is generated which stops the movement of charge carriers.

67. (c) For a wide range of values of load resistance, the current in the zener diode may change but the voltage across it remains unaffected. Thus the output voltage across the zener diode is a regulated voltage.

68. (c)

69. (d) Arsenic has five valence electrons, so it a donor impurity. Hence *X* becomes *N*-type semiconductor. Indium has only three outer electrons, so it is an acceptor impurity. Hence *Y* becomes *P*-type semiconductor. Also *N* (*i.e. X*) is connected to positive terminal of battery and *P*(*i.e. Y*) is connected to negative terminal of battery so *PN*-junction is reverse biased.

70. (a)

71. (c) In photodiode, it is illuminated by light radiations, which in turn produces electric current.

72. (a)

73. (d)

74. (d) By using $E = \frac{V}{d} = \frac{0.6}{10^{-6}} = 6 \times 10^5\ V/m$

75. (c) The given circuit is full wave rectifier.

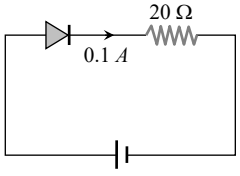
76. (a) The diode is in reverse biasing so current through it is zero.

77. (c) In full wave rectifier, the fundamental frequency in ripple is twice that of input frequency.

78. (c)

79. (c) $V = V + IR$

$= 0.5 + 0.1 \times 20$

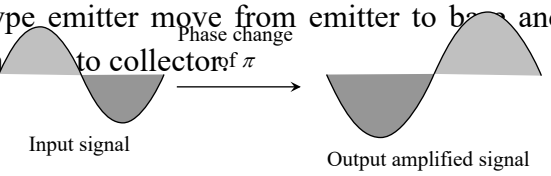


$= 2.5\ V$

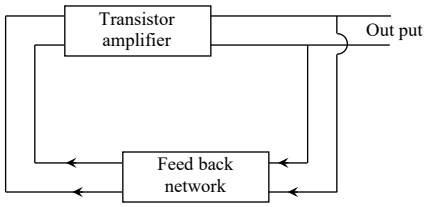
Junction Transistor

1. (a) When *NPN* transistor is used as an amplifier, majority charge carrier electrons of *N*-type emitter move from emitter to base and than to collector.

2. (c)



3. (a) In oscillator, a portion of the output power is returned back (feed back) to the input in phase with the starting power. This process is termed as positive feedback.

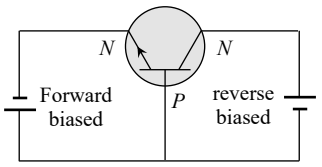


4. (d) The emitter base junction is forward biased while collector base junction is reversed biased.

5. (d) Given $i_c = \frac{80}{100} \times i_e \Rightarrow 24 = \frac{80}{100} \times i_e \Rightarrow i_e = 30\ mA$

By using $i_e = i_b + i_c \Rightarrow i_b = 30 - 24 = 6\ mA$.

6. (b)



7. (d) α is the ratio of collector current and emitter current while β is the ratio of collector current and base current.

8. (b)

9. (b) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49.$

10. (b) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24.$

11. (c) $\alpha = \frac{i_c}{i_e} = 0.96$ and $i_e = 7.2\ mA$

$\Rightarrow i_c = 0.96 \times i_e = 0.96 \times 7.2 = 6.91\ mA$

$\therefore i_e = i_c + i_b \Rightarrow 7.2 = 6.91 + i_b \Rightarrow i_b = 0.29\ mA.$

12. (d)

13. (d) $i_C = \frac{90}{100} \times i_E \Rightarrow 10 = 0.9 \times i_E = 11mA$

Also $i_E = i_B + i_C \Rightarrow i_B = 11 - 10 = 1mA$

14. (a) Current gain $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_c = \beta \times \Delta i_b = 80 \times 250\ \mu A.$

15. (b) In transistor, base is least doped.

16. (b)

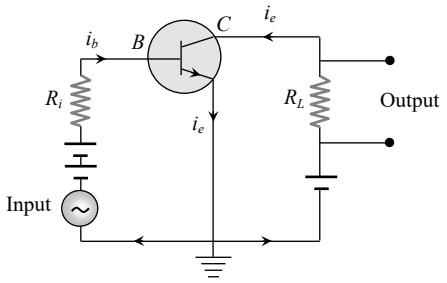
17. (d) $\beta = 50$, $R_i = 1000\ \Omega$, $V_i = 0.01V$

$\beta = \frac{i_c}{i_b}$ and $i_b = \frac{V_i}{R_i} = \frac{0.01}{10^3} = 10^{-5}\ A$

Hence $i_c = 50 \times 10^{-5}\ A = 500\ \mu A$.

18. (b) $\alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = 0.99$.

19. (a,c) The circuit of a *CE* amplifier is as shown below.



This has been shown a *NPN* transistor. Therefore base emitter are forward, biased and input signal is connected between base and emitter.

20. (a) The base is always thin

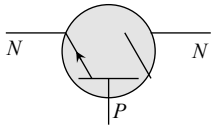
21. (c) Voltage gain = $\beta \times$ Resistance gain

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{(1-0.99)} = 99$

Resistance gain $= \frac{10 \times 10^3}{10^3} = 10$

$\Rightarrow$ Voltage gain = $99 \times 10 = 990$.

22. (a) The arrow head in the transistor symbol always shows the direction of hole flow in the emitter region.



23. (b)

24. (b) Because emitter (*N*) is common to both, base (*P*) and collector (*N*).

25. (b) Emitter is heavily doped.

26. (c) $\alpha = 0.8 \Rightarrow \beta = \frac{0.8}{(1-0.8)} = 4$

Also $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_c = \beta \times \Delta i_b = 4 \times 6 = 24mA.$

27. (a) $\Delta i_c = \alpha\, \Delta i_e = 0.98 \times 2 = 1.96\ mA$

$\therefore \quad \Delta i_b = \Delta i_e - \Delta i_c = 2 - 1.96 = 0.04\ mA$.

28. (b) $i_e = i_b + i_c \Rightarrow i_c = i_e - i_b$

29. (b) $V_b = i_b R_b \Rightarrow R_b = \frac{9}{35 \times 10^{-6}} = 257\ k\Omega.$

30. (d) $\Delta i_e = \Delta i_c + \Delta i_b$

$\Rightarrow 8 = 7.8 + \Delta i_b \Rightarrow \Delta i_b = 0.2mA = 200\ \mu$A.

31. (b) $\beta = \frac{i_c}{i_b}$

32. (b) FET is unipolar.

33. (a)

34. (b) $i_e = i_b + i_c \Rightarrow \frac{i_e}{i_c} = \frac{i_b}{i_c} + 1 \Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1 \Rightarrow \alpha = \frac{\beta}{(1+\beta)}$.

35. (b) In *NPN* transistor when emitter-base is forward biased, electrons move from emitter to base.

36. (a) Here $\Delta V_c = 0.5\ V$, $\Delta i_c = 0.05mA = 0.05 \times 10^{-3}A$

Output resistance is given by

$R_{out} = \frac{\Delta V_c}{\Delta i_c} = \frac{0.5}{0.05 \times 10^{-3}} = 10^4\ \Omega = 10k\Omega.$

37. (a) Oscillator can produce radio waves of constant amplitude.

38. (a) $h_{fe} = \left(\frac{\Delta i_c}{\Delta i_b}\right)_{V_{ce}} = \frac{8.2}{8.3 - 8.2} = 82$

39. (b) Current

gain $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_b = \frac{1 \times 10^{-3}}{100} = 10^{-5}\ A = 0.01mA.$

By using $\Delta i_e = \Delta i_b + \Delta i_c \Rightarrow \Delta i_e = 1.01 + 1 = 1.01mA.$

40. (a) In *CB* amplifier Input and output voltage signal are in same phase.

41. (b)

42. (d)

43. (d) For CE configuration voltage gain $= \beta \times R_L / R_i$

Power gain $= \beta^2 \times R_L / R_i \Rightarrow \frac{\text{Power gain}}{\text{Voltage gain}} = \beta$

44. (b) As we know $i_E = i_C + i_B$

$\Rightarrow \frac{i_e}{i_c} = 1 + \frac{i_b}{i_c} \Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \beta = \frac{\alpha}{1-\alpha}$.

Digital Electronics

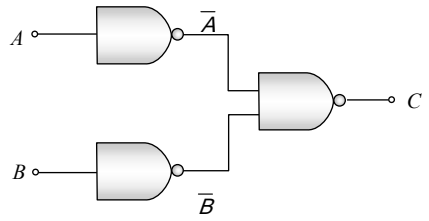
1. (b)

2. (c)

3. (b) For 'OR' gate $X = A + B$

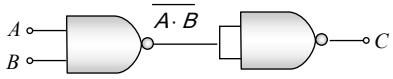
i.e. $0+0=0,\ 0+1=1,\ 1+0=1,\ 1+1=1$

4. (a)



$C = \overline{\overline{A}.\overline{B}} = \overline{\overline{A} + \overline{B}} = A + B$ (De morgan's theorem)

Hence output C is equivalent to OR gate.



$C = \overline{\overline{AB}.\overline{AB}} = \overline{\overline{AB}} + \overline{\overline{AB}} = AB + AB = AB$

In this case output C is equivalent to AND gate.

5. (b) In 'NOR' gate $Y = \overline{A + B}$

i.e. $\overline{0+0} = \overline{0} = 1,\ \overline{1+0} = \overline{1} = 0$

$\overline{0+1} = \overline{1} = 0,\ \overline{1+1} = \overline{1} = 0$

6. (c) For 'XNOR' gate $Y = \overline{A}\,\overline{B} + AB$

i.e. $\overline{0}.\overline{0} + 0.0 = 1.1 + 0.0 = 1 + 0 = 1$

$\overline{0}.\overline{1} + 0.1 = 1.0 + 0.1 = 0 + 0 = 0$

$\overline{1}.\overline{0} + 1.0 = 0.1 + 1.0 = 0 + 0 = 0$

$\overline{1}.\overline{1} + 1.1 = 0.0 + 1.1 = 0 + 1 = 1$

7. (d) The output D for the given combination

$D = \overline{(A+B).C} = \overline{(A+B)} + \overline{C}$

If $A = B = C = 0$ then

$D = \overline{(0+0)} + \overline{0} = \overline{0} + \overline{0} = 1 + 1 = 1$

If $A = B = 1,\ C = 0$ then

$D = \overline{(1+1)} + \overline{0} = \overline{1} + \overline{0} = 0 + 1 = 1$

8. (b)

9. (a) The Boolean expression for 'NOR' gate is $Y = \overline{A + B}$

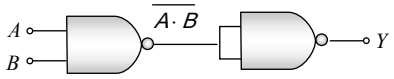
i.e. if $A = B = 0$ (Low), $Y = \overline{0+0} = \overline{0} = 1$ (High)

10. (a)

11. (d) The Boolean expression for 'AND' gate is $R = P.Q$

$\Rightarrow$1.1 = 1, 1.0 = 0, 0.1 = 0, 0.0 = 0

12. (b) Two 'NAND' gates are required as follows



$Y = \overline{\overline{AB}.\overline{AB}} = AB$

13. (c) For 'NAND' gate (option c), output $= \overline{0.1} = \overline{0} = 1$

14. (a) AND + NOT $\rightarrow$ NAND

15. (c) For 'NOT' gate $X = \overline{A}$

16. (a) The given Boolean expression can be written as

$Y = (\overline{A+B}).(\overline{A.B}) = (\overline{A}.\overline{B}).(\overline{A} + \overline{B}) = (\overline{A}\,\overline{A}).\overline{B} + \overline{A}(\overline{B}.\overline{B})$

$= \overline{A}.\overline{B} + \overline{A}\,\overline{B} = \overline{A}\,\overline{B}$

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

17. (b) For 'AND' gate, if output is 1 then both inputs must be 1.

18. (b)

19. (a)

20. (a) The given symbol is of 'AND' gate.

21. (b) It is the symbol of 'NOR' gate.

22. (c) The Boolean expression for the given combination is

output $Y = (A+B).C$

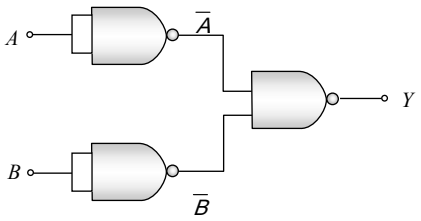
The truth table is

A	B	C	$Y = (A+B).C$
0	0	0	0

1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Hence $A=1$, $B=0$, $C=1$

23. (b)



$Y=\overline{\overline{A}.\overline{B}}=\overline{\overline{A}}+\overline{\overline{B}}=A+B$

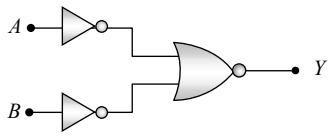
This output equation is equivalent to OR gate.

24. (c) If inputs are A and B then output for NAND gate is $Y=\overline{AB}$

$\Rightarrow$ If $A=B=1$, $Y=\overline{1.1}=\overline{1}=0$

25. (b)

26. (c)



$Y=\overline{\overline{A}+\overline{B}}$

According to De morgan's theorem

$Y=\overline{\overline{A}+\overline{B}}=\overline{\overline{A}}.\overline{\overline{B}}=A.B$

This is the output equation of 'AND' gate.

27. (b) The output of OR gate is $Y=A+B$.

28. (a) The given symbol is of NAND gate.

29. (a) $(100010)_2=2^5\times1+2^4\times0+2^3\times0+2^2\times0+2^1\times1+2^0\times0=32+0+0+0+2+0=(34)_{10}$

and $(11011)_2=2^4\times1+2^3\times1+2^2\times0+2^1\times1+2^0\times1=16+8+0+2+1=(27)_{10}$

$\therefore$ Sum $(100010)_2+(11011)_2=(34)_{10}+(27)_{10}=(61)_{10}$

Now

		Remain der
2	30	1 LSD
2	15	0
2	7	1
2	3	1
2	1	1
	0	1 MSD

$\therefore$ Required sum (in binary system) $(100010)_2+(11011)_2=(111101)_2$

30. (d) For 'NAND' gate $C=\overline{A.B}$

i.e. $\overline{0.0}=\overline{0}=1$, $\overline{0.1}=\overline{0}=1$

$\overline{1.0}=\overline{0}=1$, $\overline{1.1}=\overline{1}=0$

31. (d) 'NOR' gates are considered as universal gates, because all the gates like AND, OR, NOT can be obtained by using only NOR gates.

Valve Electronics (Diode and Triode)

1. (c) According to Richardson-Dushman equation, number of thermions emitted per sec per unit area $J=AT^2e^{-W_0/kT}\Rightarrow J\propto T^2$

2. (c) Intensity $\propto$ Number of electrons

3. (a) In SCR (Space charge region) electrons collect around the plate, this cloud decreases the emission of electrons from the cathode, hence plate current decreases.

4. (b)

5. (b) By using $g_m=\frac{\Delta i_p}{\Delta v_g}\Rightarrow 3\times10^{-4}=\frac{\Delta i_p}{-1-(-3)}$

$\Rightarrow \Delta i_p=6\times10^{-4}\,A=0.6\,mA$

6. (b) Voltage gain $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}$ and $\mu=r_p\times g_m$

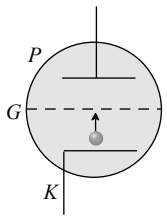
$\Rightarrow r_p=\frac{42}{2\times10^{-3}}=21000\,\Omega\Rightarrow$

$A_v=\frac{42}{1+\frac{21000}{50\times10^3}}=29.57$

7. (c) Voltage gain $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}$, for $r_p=R_L\Rightarrow$

$A_v=\frac{\mu}{2}$

8. (b) When grid is given positive potential more electrons will cross the grid to reach the positive plate *P*. Hence current increases.



9. (a) By using $\mu = -\frac{\Delta V_p}{\Delta V_g} = r_p \times g_m$

$\Rightarrow 7 \times 10^3 \times 2.5 \times 10^{-3} = -\frac{50}{\Delta V_g} \Rightarrow \Delta V_g = -2.86\ V.$

10. (a) Using voltage gain $A_v = \frac{\mu}{1+\frac{r_p}{R_L}}$ also

$\mu = r_p \times g_m$

$\Rightarrow r_p = \frac{\mu}{g_m} = \frac{20}{3 \times 10^{-3}}$

$\therefore A_v = \frac{20}{1+\frac{20}{3\times10^{-3}\times3\times10^4}} = \frac{180}{11} = 16.36.$

11. (c) Voltage gain $= \frac{V_{out}}{V_{in}} = \frac{\mu}{1+\frac{r_p}{R_L}}$

$\Rightarrow \frac{V_{out}}{0.5} = \frac{25}{1+\frac{40\times10^3}{10\times10^3}}$

$\Rightarrow V_{out} = 2.5\ V.$

12. (b) $\mu = -\frac{\Delta V_p}{\Delta V_G} \Rightarrow \Delta V_p = -\mu \Delta V_G = -20 \times (-0.2) = 4V.$

13. (b) Voltage gain $A_V = \frac{\mu}{1+\frac{r_p}{R_L}}$ and $\mu = r_p \times g_m$

$\Rightarrow \mu = 10 \times 10^3 \times 3 \times 10^{-3} = 30$

$\therefore A_v = \frac{\mu}{1+\frac{r_p}{2r_p}} = \frac{2}{3}\mu = \frac{2}{3} \times 30 = 20.$

14. (c)

15. (d) After saturation plate current can be increased by increasing the temperature of filament. It can be done by increasing the filament current.

16. (b) The maximum voltage gain $(A_v)_{max} = \mu$ (Which is obtained when $R_L = \infty$).

17. (b) Voltage gain $A_v = \frac{\mu}{1+\frac{r_p}{R_L}}$

$\because R_L = 1.5\, r_p \Rightarrow A_v = \frac{\mu}{1+\frac{r_p}{1.5\, r_p}} = \frac{3}{5}\mu = \frac{3}{5} \times 20 = 12.$

18. (c)

19. (c)

20. (c) $\mu = \frac{\Delta V_p}{\Delta V_g} \Rightarrow \Delta V_p = \mu \Delta V_g = 15 \times 0.3 = 4.5\ volt.$

21. (b) Plate resistance $= \frac{1}{\text{slope}} = \frac{1}{10^{-3}\times10^{-3}} = 10^6 \Omega$

$= 1000\ k\Omega$ (static).

22. (b) Using $A_v = \frac{\mu}{1+\frac{r_p}{R_L}}$ and $\mu = r_p \times g_m$

$\Rightarrow r_p = \frac{\mu}{g_m} = \frac{50}{2\times10^{-3}} = 25\times10^3 \Omega$

$\therefore A_v = \frac{50}{1+\frac{25\times10^3}{25\times10^3}} = 25.$

23. (b) $P = Vi \Rightarrow V = \frac{P}{i} = \frac{448\times10^{-3}}{14\times10^{15}\times1.6\times10^{-19}} = 200\ V$

24. (c) $\mu = \frac{(V_{p_1} - V_{p_2})}{(V_{G_1} - V_{G_2})} = \frac{(200-220)}{(0.5-1.3)} = 25.$

25. (a) $\mu = r_p \times g_m \Rightarrow g_m = \frac{\mu}{r_p} = \frac{22}{6600} = \frac{1}{300}.$

26. (c) $r_p = \frac{V_{p_1} - V_{p_2}}{I_{p_1} - I_{p_2}} = \frac{75-100}{(2-4)\times10^{-3}} = 12.5 \times 10^3 \Omega$

$= 12.5 k\Omega.$

27. (d)

28. (a)

29. (a) Voltage amplification $A_v = \frac{\mu}{1+\frac{r_p}{R_L}}$

$\Rightarrow \quad 25 = \frac{\mu}{1+\frac{r_p}{50\times10^3}}$ .....(i)

and $30 = \frac{\mu}{1+\frac{r_p}{100\times10^3}}$ .....(ii)

an solving equation (i) and (ii), $r_p = 25k\Omega.$

30. (a, d)

31. (d)

32. (c) Before saturation region, linear region comes. In linear region $i_p \propto V_p$

$\Rightarrow \frac{i_1}{i_2} = \frac{V_{p_1}}{V_{p_2}} = \frac{400}{200} = \frac{2}{1}$.

33. (c) $i_p = 1.125 - 1.112 = 0.013A = 13\ mA$.

34. (a)

35. (a)

36. (c) Comparing the given equation with standard equation

$i = AT^2 e^{qV/kT} \Rightarrow V_L = \frac{kT}{V}$.

37. (b)

38. (d) $r_p = \frac{\Delta V_p}{\Delta i_p} = \frac{150-100}{(12-7.5)\times 10^{-3}} = \frac{50}{4.5}\times 10^3 = 11.1k\Omega$.

39. (b)

40. (c) Voltage amplification $A_v = \frac{\mu}{1+\frac{r_p}{R_L}} = \frac{\mu R_L}{R_L + r_p}$

$\Rightarrow \frac{A_1}{A_2} = \frac{2+4}{4+4} = \frac{3}{4}$.

41. (c) A diode is used as a rectifier to convert *ac* in to *dc*.

42. (b) Fluctuating → Filter → *dc* smooth *dc*.

43. (d)

44. (b)

45. (c) $\mu = r_p \times g_m \Rightarrow r_p = \frac{20}{10^{-3}} = 2 \times 10^4 \Omega$.

46. (c)

47. (b) $\mu = -\frac{\Delta V_p}{\Delta V_g}$

$\Rightarrow \Delta V_p = -\mu \times \Delta V_g = -50(-0.20) = 10V$.

48. (b) $r_p = \frac{1}{\text{slope}} = \frac{1}{2\times 10^{-2}\times 10^{-3}} = 50k\Omega$.

49. (a) Voltage amplification

$A_v = \frac{\mu}{1+\frac{r_p}{R_L}} = \frac{r_p \times g_m \times R_L}{R_L + r_p}$

$\Rightarrow 10 = \frac{20\times 10^3 \times 2.5\times 10^{-3}\times R_L}{(R_L + 20\times 10^3)} \Rightarrow R_L = 5k\Omega$.

50. (c) Voltage gain $A_v = \frac{\mu}{1+\frac{r_p}{R_L}} = \frac{18}{1+\frac{8\times 10^3}{10^4}} = 10$.

51. (a) Ripple factor

$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{(I_0/2)^2}{(I_0/\pi)^2} - 1} = 1.21$.

52. (b)

53. (b)

54. (a) $\mu = r_p \times g_m = 2.5\times 10^4 \times 2\times 10^{-3} = 50$.

55. (c) $\mu = \left(\frac{\Delta V_p}{\Delta V_g}\right)_{i_p = \text{constant}} = \frac{(225-200)}{(5.75-5)} = 33.3$

56. (a) $g_m = \left(\frac{\Delta I_p}{\Delta V_g}\right)_{V_p = \text{constant}} = \frac{(7.5-5.5)}{-1.2-(-2.2)} = 2mmho$

57. (a)

58. (d)Using $\mu = r_p \times g_m \Rightarrow g_m = \frac{20}{10\times 10^3} = 2\times 10^{-3}$.

Critical Thinking Questions

1. (c) Number density of atoms in silicon specimen = $5 \times 10^{28}\ atom/m^3 = 5 \times 10^{22}\ atom/cm^3$

Since one atom of indium is doped in 5×10^7 *Si* atom. So number of indium atoms doped per cm^3 of silicon.

$n = \frac{5\times 10^{22}}{5\times 10^7} = 1\times 10^{15}\ atom/cm^3$.

2. (a) The probability of electrons to be found in the conduction band of an intrinsic semiconductor

$P(E) = \frac{1}{1+e^{\frac{(E-E_F)}{kT}}}$; where k = Boltzmann's constant

Hence, at a finite temperature, the probability decreases exponentially with increasing band gap.

3. (c) When donor impurity (+5 valence) added to a pure silicon (+4 valence), the +5 valence donor atom sits in the place of + 4 valence silicon atom. So it has a net additional + 1 electronic charge. The four valence electron form covalent bond and get fixed in the lattice. The fifth electron (with net – 1 electronic charge) can be approximated to revolve around + 1 additional charge. The situation is like the hydrogen atom for which energy is given by $E = -\frac{13.6}{n^2} eV$. For the case of hydrogen, the permittivity was taken as ε_0. However, if the medium has a

permittivity ε_r, relative to ε_0, then $E = -\frac{13.6}{\varepsilon_r^2 n^2} eV$

For Si, $\varepsilon_r = 12$ and for $n = 1$, $E \tilde{-} 0.1\, eV$

4. (c) The forward current

$$i = i_s(e^{eV/kT} - 1) = 10^{-5}\left[e^{\frac{1.6\times10^{-19}\times0.2}{1.4\times10^{-23}\times300}} - 1\right]$$

$$= 10^{-5}[2038.6 - 1] = 20.376\times10^{-3}\, A$$

5. (a,b,d) At 0 K, a semiconductor becomes a perfect insulator. Therefore at 0 K, if some potential difference is applied across an insulator or a semiconductor, current is zero. But a conductor will become a superconductor at 0 K. Therefore, current will be infinite. In reverse biasing at 300 K through a P-N junction diode, a small finite current flows due to minority charge carriers.

6. (a) Since diode in upper branch is forward biased and in lower branch is reversed biased. So current through circuit $i = \frac{V}{R + r_d}$; here r_d = diode resistance in forward biasing = 0

$\Rightarrow\ i = \frac{V}{R} = \frac{2}{10} = 0.2A.$

7. (a) The voltage drop across resistance = 8 – 0.5 = 7.5 V

$\therefore$ Current $i = \frac{7.5}{2.2\times10^3} = 3.4\, mA$

8. (c)

$$E = \frac{hc}{\lambda} \Rightarrow \lambda = \frac{hc}{E} = \frac{6.6\times10^{-34}\times3\times10^8}{57\times10^{-3}\times1.6\times10^{-19}} = 2$$

17100Å.

9. (b) The diode in lower branch is forward biased and diode in upper branch is reverse biased

$\therefore\quad i = \frac{5}{20+30} = \frac{5}{50} A.$

10. (b) The current through circuit $i = \frac{P}{V} = \frac{100\times10^{-3}}{0.5} = 0.2A$

$\therefore$ voltage drop across resistance = 1.5 – 0.5 = 1 V

$\Rightarrow\ R = \frac{1}{0.2} = 5\Omega.$

11. (d) In common emitter configuration current gain

$$A_i = \frac{-h_{fe}}{1 + h_{oe}R_L} = \frac{-50}{1 + 25\times10^{-6}\times10^3} = -48.78.$$

12. (c) Voltage gain $= \frac{\text{Output voltage}}{\text{Input voltage}}$

$\Rightarrow V_{out} = V_{in} \times$ Voltage gain

$\Rightarrow\ V_{out} = V_{in} \times$ Current gain $\times$ Resistance gain

$$= V_{in} \times \beta \times \frac{R_L}{R_{BE}} = 10^{-3}\times100\times\frac{10}{1} = 1V.$$

13. (a) $n_e = 8\times10^{18}/m^3,\ n_h = 5\times10^{18}/m^3$

$$\mu_e = 2.3\frac{m^2}{volt-\sec},\ \mu_h = 0.01\frac{m^2}{volt-\sec}$$

$\because n_e > n_h$ so semiconductor is N-type

Also conductivity

$$\sigma = \frac{1}{\text{Resistivity}\ (\rho)} = e(n_e\mu_e + n_h\mu_h)$$

$$\Rightarrow \frac{1}{\rho} = 1.6\times10^{-19}[8\times10^{18}\times2.3 + 5\times10^{18}\times0.01]$$

$\Rightarrow \rho = 0.34\ \Omega$-$m$.

14. (b) $V_{rms} = \frac{V_0}{2} = \frac{200}{2} = 100\, V$

15. (a) At knee point voltage across the diode is $0.7V$.

Hence voltage across resistance R is 5 – 0.7 = 4.3 V.

$\Rightarrow$ using $V = iR \Rightarrow 4.3 = 1\times10^{-3}\times R\ \Rightarrow R = 4.3\ k\Omega$.

16. (d) In positive half cycle one diode is in forward biasing and other is in reverse biasing while in negative half cycle their polarity reverses, and direction of current is opposite through R for positive and negative half cycles so out put is not rectified.

Since R_1 and R_2 are different hence the peaks during positive half and negative half of the input signal will be different.

17. (b) In half wave rectifier $V_{dc} = \frac{V_0}{\pi} = \frac{10}{\pi}$

18. (a) In common base mode $\alpha = 0.98$, $R = 5\ k\Omega$, $R_{in} = 70\Omega$

$\therefore$ voltage gain $A_v = \alpha \times \frac{R}{R_{in}} = 0.98 \times \frac{5 \times 10^3}{70} = 70$

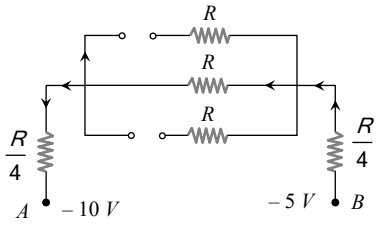
Power gain = Current gain × Voltage gain

$= 0.98 \times 70 = 68.6$

19. (a) $r_n = \varepsilon_r \left(\frac{n^2}{Z}\right) a_o = 12 \times \frac{(5^2)}{15} \times 0.53 = 10.6$ Å.

20. (c) (i) $V_A = -10V$ and $V_B = -5V$

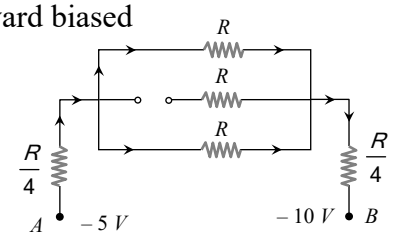
Diodes D_1 and D_3 are reveres biased and D_2 is forward biased.



$\Rightarrow R_{AB} = R + \frac{R}{4} + \frac{R}{4} = \frac{3}{2}R$.

(ii) When $V_A = -5V$ and $V_B = -10V$

Diodes D_2 is reverse biased D_1 and D_3 are forward biased



$\Rightarrow R_{AB} = \frac{R}{4} + \frac{R}{2} + \frac{R}{4} = R$.

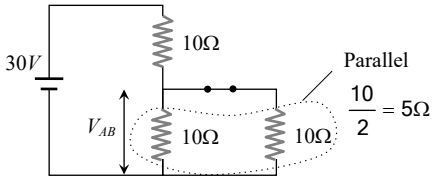
(iii) In this case equivalent resistance between A and B is also R.

Hence (ii) = (iii) < (i).

21. (b) According to the given polarity, diode D_1 is forward biased while D_2 is reverse biased. Hence current will pass through D_1 only.

So current $i = \frac{6}{(150 + 50 + 100)} = 0.02\ A$

22. (a) Diode is in forwards biasing hence the circuit can be redrawn as follows



$V_{AB} = \frac{30}{(10 + 5)} \times 5 = 10\ V$

23. (d) The diode D will conduct for positive half cycle of *a.c.* supply because this is forward biased. For negative half cycle of *a.c.* supply, this is reverse biased and does not conduct. So out put would be half wave rectified and for half wave rectified out put

$V_{rms} = \frac{V_0}{2} = \frac{200\sqrt{2}}{2} = \frac{200}{\sqrt{2}}$

24. (d) $\sigma = ne(\mu_e + \mu_h) = 2 \times 10^{19} \times 1.6 \times 10^{-19}(0.36 + 0.14)$

$= 1.6\ (\Omega - m)^{-1}$

$R = \rho \frac{l}{A} = \frac{l}{\sigma A} = \frac{0.5 \times 10^{-3}}{1.6 \times 10^{-4}} = \frac{25}{8}\Omega$

$\therefore\ i = \frac{V}{R} = \frac{2}{25/8} = \frac{16}{25}\ A = 0.64\ A$

25. (a) As we know current density $J = nqv$

$\Rightarrow J_e = n_e q v_e$ and $J_h = n_h q v_h$

$\Rightarrow \frac{J_e}{J_h} = \frac{n_e}{n_h} \times \frac{v_e}{v_h} \Rightarrow \frac{3/4}{1/4} = \frac{n_e}{n_h} \times \frac{5}{20} \Rightarrow \frac{n_e}{n_h} = \frac{6}{5}$

26. (b) Consider the case when *Ge* and *Si* diodes are connected as show in the given figure.

Equivalent voltage drop across the combination *Ge* and *Si* diode = 0.3 *V*

$\Rightarrow$ Current $i = \frac{12 - 0.3}{5\ k\Omega} = 2.34\ mA$

$\therefore$ Out put voltage $V_0 = Ri = 5\ k\Omega \times 2.34\ mA$

$= 11.7\ V$

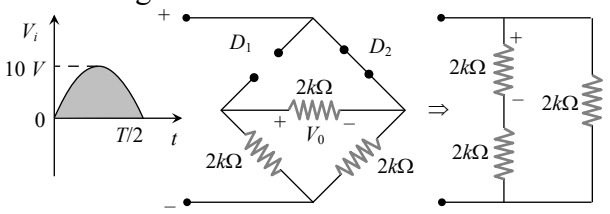
Now consider the case when diode connection are reversed. In this case voltage drop across the diode's combination = 0.7 *V*

$\Rightarrow$ Current $i = \dfrac{12 - 0.7}{5\ k\Omega} = 2.26\ mA$

$\therefore\ V_0 = iR = 2.26\ mA \times 5\ k\Omega = 11.3\ V$

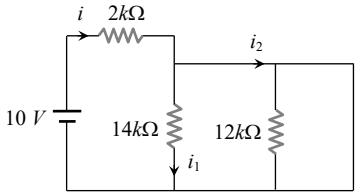
Hence charge in the value of V_0 = 11.7 – 11.3 = 0.4 V

27. (b) For the positive half cycle of input the resulting network is shown below



$\Rightarrow (V_0)_{max} = \dfrac{1}{2}(V_i)_{max} = \dfrac{1}{2} \times 10 = 5\ V.$

28. (d) The equivalent circuit can be redrawn as follows



From figure it is clear that current drawn from the battery $i = i_2 = \dfrac{10}{2} = 5mA$ and $i_1 = 0.$

29. (c) $i_b = \dfrac{5 - 0.7}{8.6} = 0.5\ mA \Rightarrow I_c = \beta\, I_b = 100 \times 0.5\ mA$

By using $V_{CE} = V_{CC} - I_c R_L = 18 - 50 \times 10^{-3} \times 100 = 13\ V$

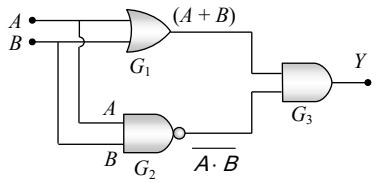
30. (a) $I_e = 10^{10} \times 1.6 \times 10^{-19} \times \dfrac{1}{10^{-6}} = 1.6\ mA \quad \left(\because I = \dfrac{Q}{t}\right)$

Since 2% electrons are absorbed by base, hence 98% electrons reaches the collector *i.e.* $\alpha = 0.98$

$\Rightarrow\ I_c = \alpha I_e = 0.98 \times 1.6 = 1.568\ mA \approx 1.57\ mA$

Also current amplification factor $\beta = \dfrac{\alpha}{1 - \alpha} = \dfrac{0.98}{0.02} = 49$

31. (b)



$Y = (A + B).\overline{AB}$

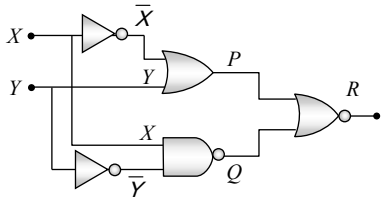
The given output equation can also be written as

$Y = (A + B).(\overline{A} + \overline{B})$ (De morgan's theorem)

$= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} = 0 + A\overline{B} + \overline{A}B + 0 = \overline{A}B + A\overline{B}$

This is the expression for XOR gate.

32. (c)

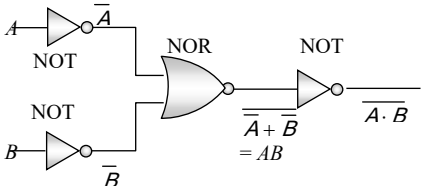


The truth table can be written as

X	Y	$\overline{X}$	$\overline{Y}$	$P = \overline{X} + Y$	$Q = \overline{X.\overline{Y}}$	$R = \overline{P + Q}$
0	1	1	0	1	1	0
1	1	0	0	1	1	0
1	0	0	1	0	0	1
0	0	1	1	1	1	0

Hence $X = 1$, $Y = 0$ gives output $R = 1$

33. (d)



Hence option (d) is correct.

34. (b) The truth table of the circuit is given

A	B	C	$X = \overline{AB}$	$Y = \overline{BC}$	$Z = \overline{X + Y}$
0	0	0	1	1	0
1	0	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0
0	1	1	1	0	0
1	1	1	0	0	1

Output Z of single three input gate is that of AND gate.

35. (c) Output of upper OR gate = $W + X$

Output of lower OR gate = $W + Y$

Net output $F = (W + X)(W + Y)$

$= WW + WY + XW + XY$ (Since $WW = W$)

$= W(1 + Y) + XW + XY$ (Since $1 + Y = 1$)

$= W + XW + XY = W(1 + X) + XY = W + XY$

36. (b) $\mu = r_p\, g_m = 50$

From $i_p = KV_p^{3/2} \Rightarrow \dfrac{\Delta V_p}{\Delta i_p} = r_p = \dfrac{2i_p^{-1/3}}{3K^{2/3}}$

$\Rightarrow \quad g_m = \dfrac{\mu}{r_p} = \dfrac{3\mu K^{2/3} i_p^{1/3}}{2}$

$= \dfrac{3}{2}\mu K^{2/3}\left[K^{1/3}(V_p + \mu V_g)^{1/2}\right]$

$= \dfrac{3}{2}\mu K(V_p + \mu V_g)^{1/2} = 75\ K\ (i_p/K)^{1/3}$

Because i_p was in mA, g_m is substituted as 5 $m\mho$

$\Rightarrow 5 = 75K^{2/3} i_p^{1/3} = 75\,K^{2/3}(8)^{1/3} \Rightarrow K = \left(\dfrac{1}{30}\right)^{3/2}$

Cut off grid voltage $V_G = -\dfrac{V_p}{\mu} = -\dfrac{300}{50} = -6\,V$

37. (d) $g_m = \left(\dfrac{\Delta i_p}{\Delta V_g}\right)_{V_p = \text{constant}} = \dfrac{(15-10)\times 10^{-3}}{0-(-4)} = 1.25\times 10^{-3}\Omega$

$\mu = \left(\dfrac{\Delta V_p}{\Delta V_g}\right)_{I_p = \text{constant}} = \dfrac{150-120}{0-(-4)} = 7.5$

$\therefore\ r_p = \dfrac{\mu}{g_m} = \dfrac{7.5}{1.25\times 10^{-3}} = 6000\ ohms$

38. (d) The dynamic plate resistance is $r_p = \dfrac{\Delta V_p}{\Delta i_p}$

Now for a vacuum diode $i_p = KV_p^{3/2} \Rightarrow V_p = \left(\dfrac{i_p}{K}\right)^{2/3}$

$\Rightarrow \dfrac{\Delta V_p}{\Delta i_p} = \dfrac{2}{3K^{2/3}} i_p^{\left(\frac{2}{3}-1\right)}$

$\Rightarrow r_p = (\text{constant}) I_p^{-1/3} \Rightarrow r_p \propto \dfrac{1}{I_p^{1/3}}$

39. (d) $i_p = [0.125\ V_p - 7.5]\times 10^{-3}\ amp$

Differentiating this equation *w.r.t.* V_p

$\dfrac{\Delta i_p}{\Delta V_p} = 0.125\times 10^{-3}$ or $\dfrac{1}{r_p} = 0.125\times 10^{-3} \Rightarrow$

$r_p = 8\ k\Omega$

40. (b) $V_{peak} = \sqrt{2}\quad V_{rms} = \sqrt{2}\times 141.4 = 200\ V$

41. (c) The emission current $i = AT^2 Se^{-\phi/kT}$

For the two surfaces $A_1 = A_2$, $S_1 = S_2$, $T_1 = 800\ K$, $T_2 = 1600\ K, \phi_1 / T_1 = \phi_2 / T_2$

Therefore, $\dfrac{i_2}{i_1} = \left(\dfrac{T_2}{T_1}\right)^2 = (2)^2 = 4 \Rightarrow$

$i_2 = 4i_1 = 4\ mA.$

42. (a) The first data gives value of plate resistance

$r_p = \dfrac{\Delta V_p}{\Delta i_p} = \dfrac{10}{0.8\times 10^{-3}} = \dfrac{10^5}{8}\Omega$

Also $g_m = \dfrac{\Delta i_p}{\Delta V_g}$ and $g_m = \dfrac{\mu}{r_p}$

$\Rightarrow \Delta V_g = \dfrac{\Delta i_p \times r_p}{\mu} = \dfrac{4\times 10^{-3}\times 10^5/8}{8} = 6.25\ V$

43. (a) $I_p = 0.004\,(V_p + 10\,V_g)^{3/2}$

$\Rightarrow \dfrac{\Delta I_p}{\Delta V_g} = 0.004\left[\dfrac{3}{2}(V_p + 10\,V_g)^{1/2}\times 10\right]$

$\Rightarrow g_m = 0.004\times\dfrac{3}{2}(120 + 10\times -2)^{1/2}\times 10$

$\Rightarrow g_m = 6\times 10^{-4}\ mho = 0.6\ m\,mho$

Comparing the given equation of I_p with standard equation $I_p = K(V_p + \mu V_g)^{3/2}$ we get $\mu = 10$

Also from $\mu = r_p \times g_m \Rightarrow r_p = \dfrac{\mu}{g_m} = \dfrac{10}{0.6\times 10^{-3}}$

$\Rightarrow r_p = 16.67\times 10^3\Omega = 16.67\ k\Omega.$

44. (b) $\mu = r_P \times g_m = 20\times 2.5 = 50$

From $A = \dfrac{\mu R_L}{r_P + R_L} \Rightarrow$

$r_P + R_L = \dfrac{\mu R_L}{A} = \dfrac{50R_L}{10} = 5R_L$

$\Rightarrow 4R_L = r_p \Rightarrow R_L = \dfrac{r_p}{4} = \dfrac{20}{4} = 5k\Omega$

45. (a) $A = \dfrac{\mu R_L}{r_p + R_L} = \dfrac{14\times 12}{10+12} = \dfrac{84}{11}$. Peak value of output signal $V_0 = \dfrac{84}{11}\times 2\sqrt{2}\,V \Rightarrow$

$V_{rms} = \dfrac{V_0}{\sqrt{2}} = \dfrac{84\times 2}{11}\,V$

$\Rightarrow$ *r.m.s.* value of current through the load

$= \dfrac{84\times 2}{11\times 12\times 10^3}\,A = 1.27\ mA$

46. (c) $r_p = \frac{\mu}{g_m} = \frac{64}{1600 \times 10^{-6}} = 4 \times 10^4 \Omega$

Voltage gain $A_v = \frac{\mu}{1 + \frac{r_p}{R_L}} = \frac{64}{1 + \frac{4 \times 10^4}{40 \times 10^3}} = 32$

$\therefore$ Output signal voltage

$V_0 = A_v \times V_i = 32 \times 1 = 32\ V(r.m.s)$

Signal power in load $= \frac{V_0^2}{R_L} = \frac{(32)^2}{40 \times 10^3} = 25.6\ mW$

47. (a) $i_p = k(V_p + \mu V_g)^{3/2}\ mA$

$\Rightarrow 4 = k(200 - 10 \times 4)^{3/2} = k \times (160)^{3/2}$ ....(i)

and $i_p = k(160 - 10 \times 7)^{3/2} = k \times (90)^{3/2}$ ....(ii)

From equation (i) and (ii) we get

$i_p = 4 \times \left(\frac{90}{160}\right)^{3/2} = 4 \times \left(\frac{3}{4}\right)^3 = 1.69\ mA$

48. (a) At $V_g = -3\ V, V_p = 300\ V$ and $I_p = 5 mA$

At $V_g = -1 V,$ for constant plate current *i.e.* $I_p = 5 mA$

From $I_p = 0.125\ V_p - 7.5$

$\Rightarrow 5 = 0.125 V_p - 7.5 \Rightarrow V_p = 100 V$

$\therefore$ change in plate voltage

$\Delta V_p = 300 - 100 = 200 V$

Change in grid voltage $\Delta V_g = -1 - (-3) = 2 V$

So, $\mu = \frac{\Delta V_p}{\Delta V_g} = \frac{200}{2} = 100$

49. (b) The slope of anode characteristic curve $= \frac{1}{r_p}$

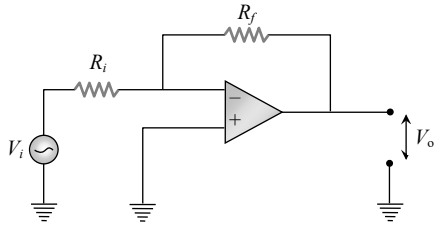
$\Rightarrow r_p = \frac{1}{0.02\ mA/\ V} = 50 \frac{V}{mA} = 50 \times 10^3 \frac{V}{A}$

The slope of mutual characteristic curve = g_m

$= 1 \times 10^{-3}\ A/V.$

$\therefore \mu = r_p \times g_m = 50 \times 10^3 \times 10^{-3} = 50$.

50. (b) Voltage gain $A = \frac{V_o}{V_i} = \frac{R_f}{R_i} = \frac{100\ k\Omega}{1\ k\Omega} = 100$.



Graphical Questions

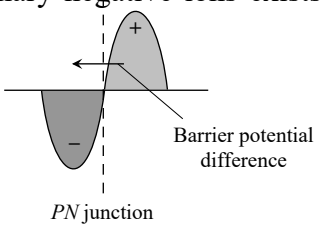
1. (c) With rise in temperature, resistivity of semiconductors decreases exponentially.

2. (b) Potential across the *PN* junction varies symmetrically linear, having *P* side negative and *N* side positive.

3. (c) *PN* junction has low resistance in one direction of potential difference $+V$, so a large current flows (forward biasing). It has a high resistance in the opposite potential difference direction $-V$, so a very small current flows (Reverse biasing).

4. (c) When input voltage is $-10\ V$, the diode is reverse biased and no output is obtained. On the other hand, when input is $+10V$, the diode is forward biased and output is obtained which is $+10V$. Therefore the output is of the form as show in the following figure.

5. (a) In the depletion layer of *PN* junction, stationary, positive ions exists in the *N*-side and stationary negative ions exists in the *P* side.



6. (b) V_k = knee voltage = 0.3 V

$\therefore$ Resistance

$= \frac{\Delta V}{\Delta i} = \frac{(2.3 - 0.3)}{(10 - 0) \times 10^{-3}} = 200\Omega = 0.2 k\Omega$

7. (b) Half wave rectifier, rectifies only the half cycle of input ac signal and it blocks the other half.

8. (c) As *RC* time constant of the capacitor is quite large ($\tau = RC = 10 \times 10^3 \times 10 \times 10^{-6} = 0.1\ sec$),

if will not discharge appreciably. Hence voltage remains nearly constant.

9. (b) In the positive half cycle of input *ac* signal diode D_1 is forward biased and D_2 is reverse biased so in the output voltage signal, *A* and *C* are due to D_1. In negative half cycle of Input *ac* signal D_2 conducts, hence output signals *B* and *D* are due to D_2.

10. (a) If *i* is the current in the diode and *V* is voltage drop across it, then for given figure voltage equation is

$$i\times 100 + V = 8 \Rightarrow i = -\frac{1}{100}V + \frac{8}{100} \Rightarrow$$

$$i = -(0.01)V + 0.08$$

Thus the slope of *i-V* graph $= \frac{1}{R_L} = 0.01$

11. (b) The current at $2V$ is 400 *mA* and at 2.1 *V* it is 800 *mA*. The dynamic resistance in this region $R = \frac{\Delta V}{\Delta i} = \frac{(2.1-2)}{(800-400)\times 10^{-3}} = \frac{1}{4} = 0.25\Omega$

12. (a) From the given waveforms, the following truth table can be made

Time interval	Inputs		Output
	A	*B*	*Y*
$0 \to T_1$	0	0	0
$T_1 \to T_2$	0	1	0
$T_2 \to T_3$	1	0	0
$T_3 \to T_4$	1	1	1

This truth table is equivalent to 'AND' gate.

13. (d) 5 *volt* is low signal (0) and 10 *volt* is high signal (1) and taking 5 μ-*sec* as 1 unit. In a negative logic, low signal (0) gives high output (1) and high signal (1) gives low output (0). The output is therefore 1010010111.

14. (a) $g_m = \frac{\Delta i_p}{\Delta V_g} = \frac{(20-15)\times 10^{-3}}{(4-2)} = 2.5$ *milli mho*

15. (d) The cut off grid voltage is that negative grid bias corresponding to which the plate current becomes zero. At point *P*, $i_p = 0$

16. (a) According to Richardson-Dushman equation $J = AT^2 e^{-b/T}$

Taking log of this equation $\log_e \frac{J}{T^2} = \log_e A - \frac{b}{T}$

i.e. graph between $\log_e \frac{J}{T^2}$ and $\frac{1}{T}$ will be a straight line having negative slope and positive intercept ($\log_e A$) on $\log_e \frac{J}{T^2}$ axis.

17. (c) $J = AT^2 e^{-b/T} \Rightarrow \frac{J}{T^2} \propto e^{-b/T}$

i.e. $\frac{J}{T^2}$ will vary exponentially with $\frac{1}{T}$, having negative slope.

18. (c) This is the graph between i_p and V_g and i_p becomes zero at certain negative potential.

19. (a) $\mu = -\left(\frac{\Delta V_p}{\Delta V_g}\right)_{\Delta i_p = \text{const.}} = \frac{-(80-60)}{[-6-(-4)]} = \frac{20}{2} = 10$

20. (c) According to $|A_v| = \frac{\mu}{1+\frac{r_p}{R_L}}$

as R_L increases A_v also increases. When R_L becomes too high then A_v = maximum = μ

Hence only option (*c*) is correct.

21. (c) With rise in temperature, work function decreases (non-linearly).

22. (c) $R_p = \frac{V_p}{i_p} = \frac{50}{150\times 10^{-3}} = 333.3\,\Omega$

23. (a) $i \propto T^2 \Rightarrow \frac{i}{i_0} = \left(\frac{T}{T_0}\right)^2$

This is the equation of a parabola.

24. (b) The band width is defined as the frequency band in which the amplifier gain remains above $\frac{1}{\sqrt{2}} = 0.707$ of the mid frequency gain (A_{max}). The low frequency f_1 at which the gain falls to $\frac{1}{\sqrt{2}}$ *i.e.* 0-.707 times it's mid frequency value is called lower cut off frequency and the high frequency f_4 at which the gain falls to $\frac{1}{\sqrt{2}}$ *i.e.* 0.707 times of it's mid frequency is known as higher cut off frequency so band width = $f_4 - f_1$.

25. (c) r_p varies with i_p according to relation $r_p \propto i_p^{-1/3}$ *i.e.* when i_p increases, r_p decreases, hence graph *C* represents the variation of r_p.

μ doesn't depends upon i_p, hence graph A is correct.

26. (c) From the graph it is clear that of for $V_g = -4\,V, i_p = 0,$ so cut off voltage is -4 *volt*.

27. (b) As temperature increases saturation current also increases.

28. (c)

29. (a) Output signal voltage has phase difference of 180° with respect to input.

30. (d) Grid is maintained between 0 *volt* to certain negative voltage.

Assertion and Reason

1. (d) In diode the output is in same phase with the input therefore it cannot be used to built NOT gate.

2. (a) According to law of mass action, $n_i^2 = n_e n_h$. In intrinsic semiconductors $n_i = n_e = n_h$ and for *P*-type semiconductor n_e would be less than n_i, since n_h is necessarily more than n_i.

3. (c) In common emitter transistor amplifier current gain $\beta > 1,$ so output current > Input current, hence assertion is correct.

Also, input circuit has low resistance due to forward biasing to emitter base junction, hence reason is false.

4. (a) Input impedance of common emitter configuration

$$= \frac{\Delta V_{BE}}{\Delta i_B}\bigg|_{V_{CE}=\text{constant}}$$

where $\Delta V_{BE} =$ voltage across base and emitter (base emitter region is forward biased)

$\Delta i_B =$ base current which is order of few microampere.

Thus input impedance of common emitter is low.

5. (d) Resistivity of semiconductors decreases with temperature. The atoms of a semiconductor vibrate with larger amplitudes at higher temperatures there by increasing it's conductivity not resistivity.

6. (a) In semiconductors the energy gap between conduction band and valence band is small (≈ 1 *eV*). Due to temperature rise, electron in the valence band gained thermal energy and may jump across the small energy gap, goes in to the conduction band. Thus conductivity increases and hence resistance decreases.

7. (b)

8. (a) The ratio of the velocity to the applied field is called the mobility. Since electron is lighter than holes, they move faster in applied field than holes.

9. (b)

Intrinsic semiconduct (Neutral + Pentalvalen impurity (Neutral → *N*-type semiconduct (Neutral

10. (a) At a particular temperature all the bonds of crystalline solids breaks and show sharp melting point.

11. (c) The energy gap for germanium is less $(0.72\,eV)$ than the energy gap of silicon $(1.1\,eV)$. Therefore, silicon is preferred over germanium for making semiconductor devices.

12. (e) We cannot measure the potential barrier of a *PN*-junction by connecting a sensitive voltmeter across its terminals because in the depletion region, there are no free electrons and holes and in the absence of forward biasing, *PN*- junction offers infinite resistance.

13. (e) The assertion is not true. In fact, semiconductor Obeys Ohm's law for low values of electric field (~ 10^6 *V/m*). Above this, the current becomes almost independent of electric field.

14. (d) Two *PN*-junctions placed back to back cannot work as *NPN* transistor because in transistor the width and concentration of doping of *P*-semiconductor is less as compared to width doping of *N*-type semiconductor type.

15. (b) Common emitter is prepared over common base because all the current, voltage and power gain of common emitter amplifier is much more than the gains of common base amplifier.

16. (d) In *PN*-junction, the diffusion of majority carriers takes place when junction is forward biased and drifting of minority carriers takes place across the function,

when reverse biased. The reverse bias opposes the majority carriers but makes the minority carriers to cross the *PN*-junction. Thus the small current in μA flows during reverse bias.

17. (d) A transistor is a current operating device because the action of transistor is controlled by the charge carriers (electrons or holes). Base current is very much lesser than the collector current.

18. (a) These gates are called digital building blocks because using these gates only (either NAND or NOR) we can compile all other gates also (like OR, AND, NOT, XOR).

19. (d) At $0K$, Germanium offers infinite resistance, and it behaves as an insulator.

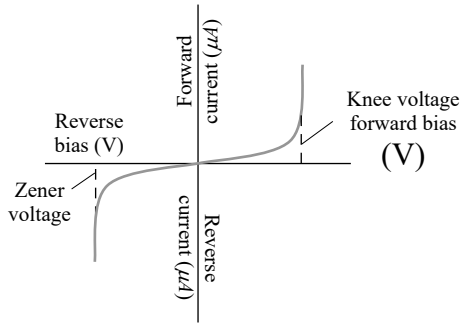
20. (a) In a transistor, the base is made extremely thin to reduce the combinations of holes and electrons. Under this condition, most of the holes (or electrons) arriving from the emitter diffuses across the base and reach the collector. Hence, the collector current, is almost equal to the emitter current, the base current being comparatively much smaller. This is the main reason that power gain and voltage gain are obtained by a transistor. If the base region was made quite thick, then majority of carriers from emitter will combine with the carriers in the base and only small number of carriers will reach the collector, so there would be little collector current and the purpose of transistor would be defeated.

21. (c) The current gain in common base circuit $\alpha = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_C}$

The change in collector current is always less than the change in emitter current.

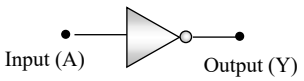
$\Delta I_C < \Delta I_E$. Therefore, $\alpha < 1$.

22. (d) The *V-i* characteristic of *PN*- diode depends whether the junction is forward biased or reverse biased. This can be showed by graph between voltage and current.



23. (a) When the reverse voltage across the zener diode is equal to or more than the breakdown voltage, the reverse current increases sharply.

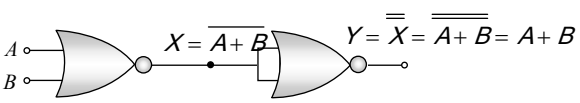
24. (a)



If $A = 0$, $Y = 1$ and $A = 1$, $Y = 0$.

25. (b) In vacuum tubes, vacuum is necessary and the working of semiconductor devices is independent of heating or vacuum.

26. (a)



This is the Boolean expression for 'OR' gate.

27. (a) For detection of a particular wavelength (λ) by a *PN* photo diode, energy of incident light > $E_g \Rightarrow \frac{hc}{E_g} > \lambda$

For

$$E_g = 2.8\ eV, \frac{hc}{E_g} = \frac{6.6\times10^{-34}\times3\times10^{8}}{2.8\times1.6\times10^{-19}} = 441.9\ nm$$

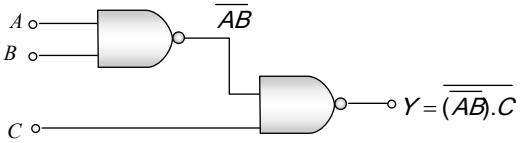
i.e. $\frac{hc}{E_g} < 6000\ nm$, so diode will not detect the wavelength of 6000Å.

28. (a)

29. (b) In forward biasing of *PN* junction current flows due to diffusion of majority charge carriers. While in reverse biasing current flows due to drifting of minority charge carriers.

The circuit given in the reason is a *PNP* transistor having emitter is more negative *w.r.t.* base so it is reverse biased and collector is more positive *w.r.t.* base so it is forward biased.

30. (c) Assertion is true but reason is false



If $A = 1, B = 0, C = 1$ then $Y = 0$

31. (b) Both assertion and reason are true but potential difference across the resistance is zero, because diode is in reverse biasing hence no current flows.