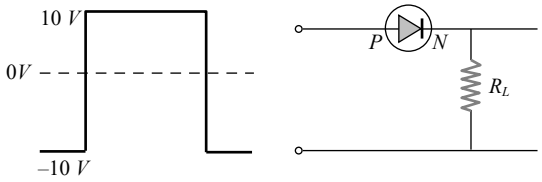
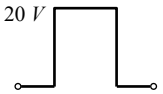
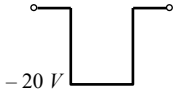
4. If the following input signal is sent through a *PN*-junction diode, then the output signal across R_L will be



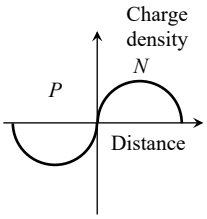
(a) 

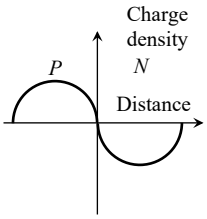
(b) 

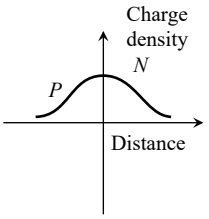
(c) 

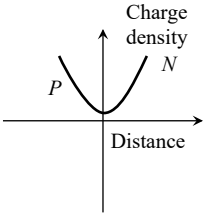
(d) 

5. The curve between charge density and distance near *P-N* junction will be

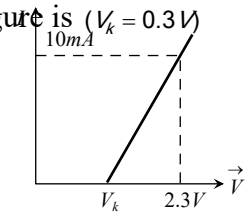
(a) 

(b) 

(c) 

(d) 

6. The resistance of a germanium junction diode whose $V-I$ is shown in figure is $(V_k = 0.3\,V)$



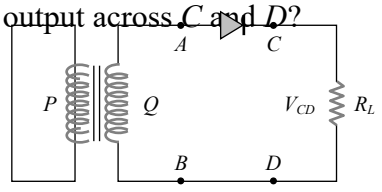
(a) 5 $k\Omega$

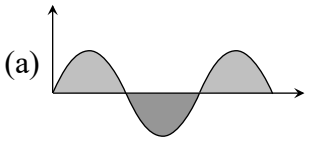
(b) 0.2 $k\Omega$

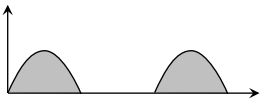
(c) 2.3 $k\Omega$

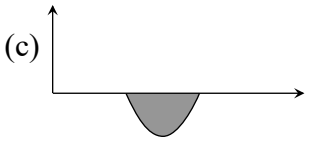
(d) $\left(\frac{10}{2.3}\right)k\Omega$

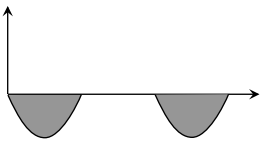
7. In the half-wave rectifier circuit shown. Which one of the following wave forms is true for V_{CD}, the output across *C* and *D*?



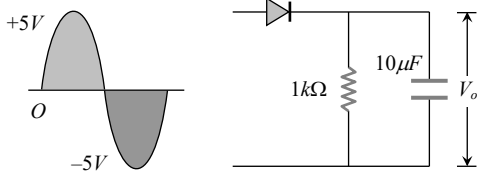
(a) 

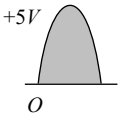
(b) 

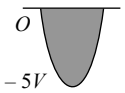
(c) 

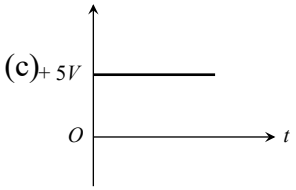
(d) 

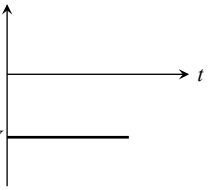
8. The output in the circuit of figure is taken across a capacitor. It is as shown in figure



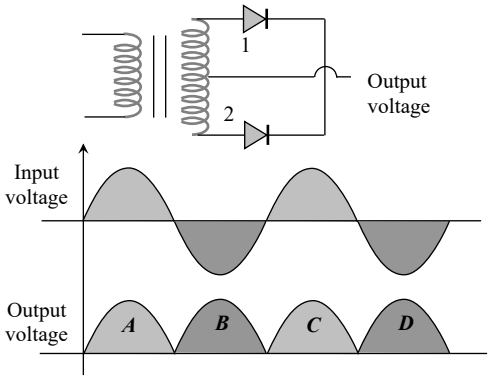
(a) 

(b) 

(c) 

(d) 

9. A full wave rectifier circuit along with the input and output voltages is shown in the figure



The contribution to output voltage from diode – 2 is

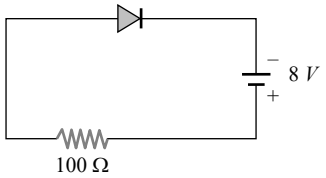
[MP PMT 2001]

(a) *A*, *C* (b) *B*, *D*

(c) *B*, *C* (d) *A*, *D*

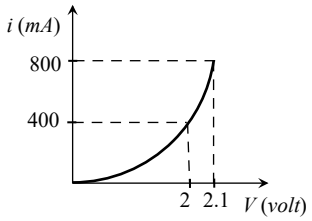
10. A source voltage of 8*V* drives the diode in fig. through a current-limiting resistor of 100 *ohm*.

Then the magnitude of the slope load line on the *V-I* characteristics of the diode is



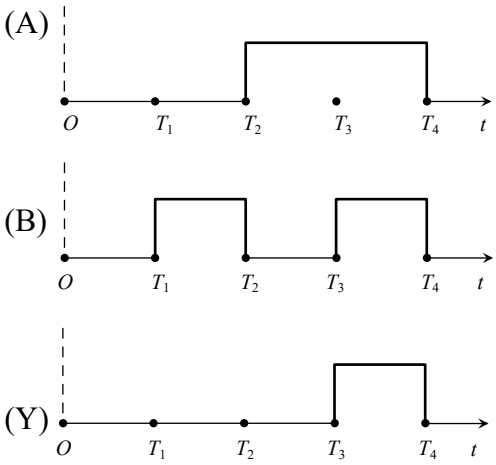
(a) 0.01
(b) 100
(c) 0.08
(d) 12.5

11. The *i-V* characteristic of a *P-N* junction diode is shown below. The approximate dynamic resistance of the *P-N* junction when a forward bias of 2*volt* is applied



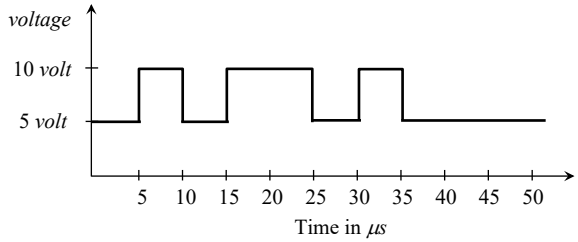
(a) 1 Ω
(b) 0.25 Ω
(c) 0.5 Ω
(d) 5 Ω

12. The given figure shows the wave forms for two inputs *A* and *B* and that for the output *Y* of a logic circuit. The logic circuit is



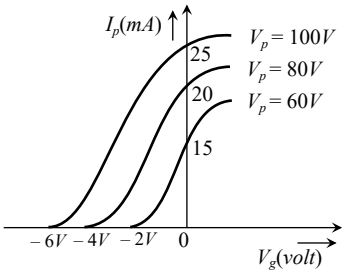
(a) An AND gate
(b) An OR gate
(c) A NAND gate
(d) An NOT gate

13. In a negative logic the following wave form corresponds to the



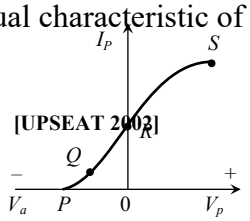
(a) 0000000000
(b) 0101101000
(c) 1111111111
(d) 1010010111

14. The variation of anode current in a triode corresponding to a change in grid potential at three different values of the plate potential is shown in the diagram. The mutual conductance of the triode is **[CPMT 1986, 88]**



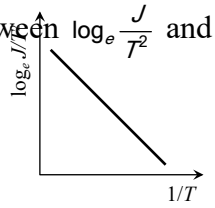
(a) 2.5 *m mho*
(b) 5.0 *m mho*
(c) 7.5 *m mho*
(d) 10.0 *m mho*

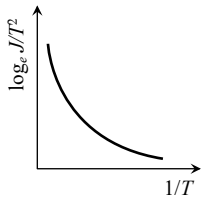
15. The point representing the cut off grid voltage on the mutual characteristic of triode is **[UPSEAT 2003]**

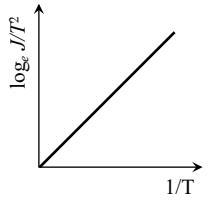


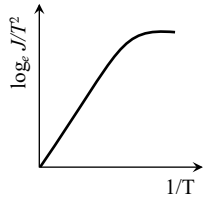
(a) *S*
(b) *R*
(c) *O*
(d) *P*

16. For a thermionic emitter (metallic) if *J* represents the current density and *T* is its absolute temperature then the correct curve between $\log_e \frac{J}{T^2}$ and $\frac{1}{T}$ is

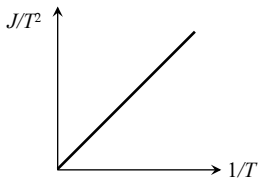
(a) 

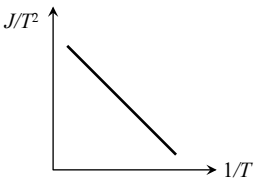
(b) 

(c) 

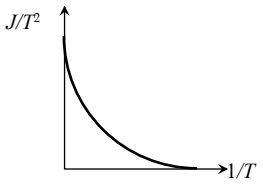
(d) 

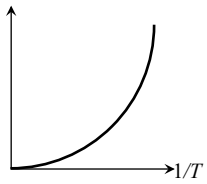
17. If the thermionic current density is *J* and emitter temperature is *T* then the curve between $\frac{J}{T^2}$ and $\frac{1}{T}$ will be



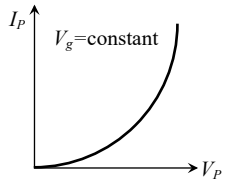


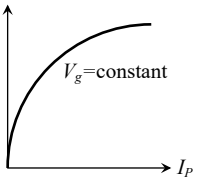
(a) (b)

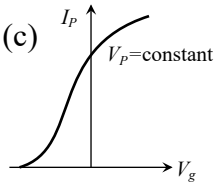
(c) 

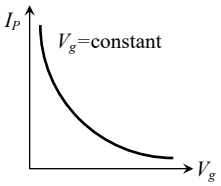
(d) 

18. The mutual characteristic of triode is

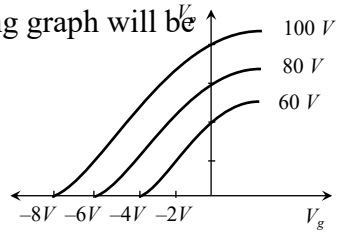
(a) 

(b) 

(c) 

(d) 

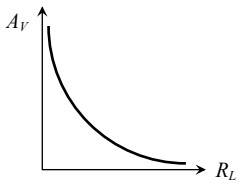
19. The value of amplification factor from the following graph will be

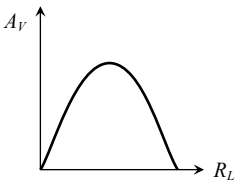


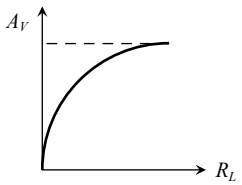
(a) 10 (b) 50

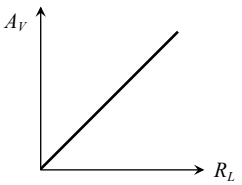
(c) 25 (d) 40

20. The correct curve between voltage gain (A_v) and load resistance (R_L) is

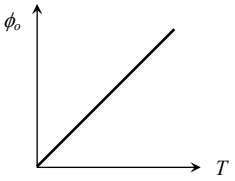
(a) 

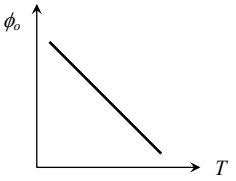
(b) 

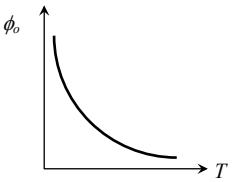
(c) 

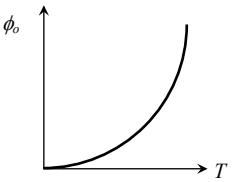
(d) 

21. The curve between the work function of a metal (ϕ_o) and its temperature (T) will be

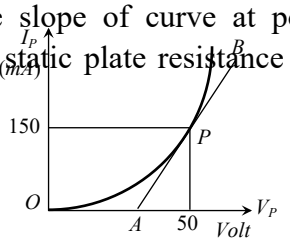
(a) 

(b) 

(c) 

(d) 

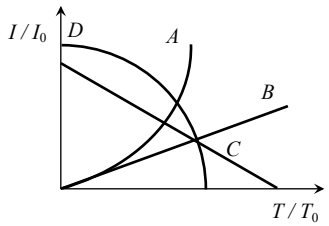
22. The plate characteristic curve of a diode in space charge limited region is as shown in the figure. The slope of curve at point P is 5.0 mA/V. The static plate resistance of diode will be



(a) 111.1Ω (b) 222.2Ω

(c) 333.3Ω (d) 444.4Ω

23. The ratio of thermionic currents (I/I_0) for a metal when the temperature is slowly increased T_0 to T as shown in figure. (I and I_0 are currents at T and respectively). Then which one is correct? **[Orissa JEE 2002]**

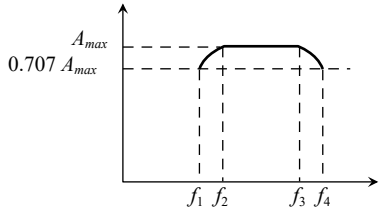


(a) A (b) B

(c) C (d) D

24. The frequency response curve of RC coupled

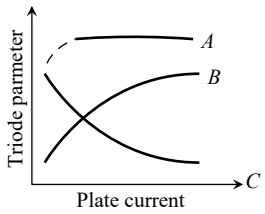
amplifier is shown in figure. The band width of the amplifier will be



(a) $f_3 - f_2$ (b) $f_4 - f_1$

(c) $\frac{f_4 - f_2}{2}$ (d) $f_3 - f_1$

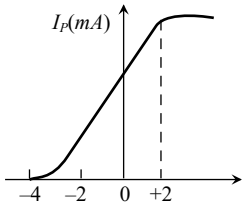
25. The figure represents variation of triode parameter (μ or r_p or g_m) with the plate current. The correct variation of μ and r_p are given, respectively by the curves



(a) *A* and *B* (b) *B* and *C*

(c) *A* and *C* (d) None of the above

26. The mutual characteristic curves of a triode are as shown in figure. The cut off voltage for the triode is

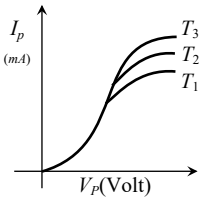


(a) 0 *V* (b) 2 *V*

(c) – 4 *V* (d) 6 *V*

27. For the diode, the characteristic curves are given at different temperature. The relation between the temperatures is

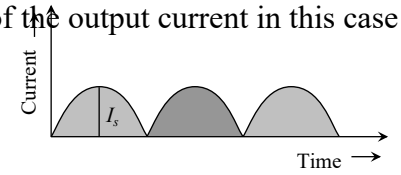
[RPET 1990]



(a) $T_1 = T_2 = T_3$ (b) $T_1 < T_2 < T_3$

(c) $T_1 > T_2 > T_3$ (d) None of the above

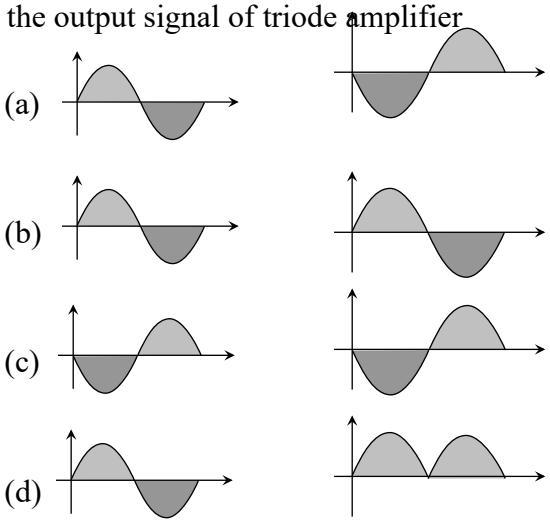
28. The output current versus time curve of a rectifier is shown in the figure. The average value of the output current in this case is



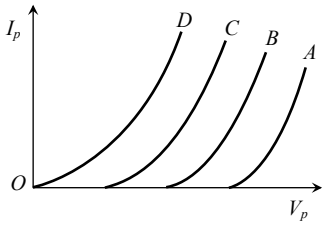
(a) 0 (b) i_0/π

(c) $2i_0/\pi$ (d) i_0

29. Which of the following figures correctly shows the phase relation between the input signal and the output signal of triode amplifier



30. In the figure four plate characteristics of a triode at different grid voltage are shown. The difference between successive grid voltage is 1 *V*. Which curve will have maximum grid voltage and what is its value?



(a) *A*, $V_g = +4$ *V* (b) *B*, $V_g = +4$ *V*

(c) *A*, $V_g = 0$ (d) *D*, $V_g = 0$

Read the assertion and reason carefully to mark the correct option out of the options given below:

(a) If both assertion and reason are true and the reason is the correct explanation of the assertion.
(b) If both assertion and reason are true but reason is not the correct explanation of the assertion.
(c) If assertion is true but reason is false.
(d) If the assertion and reason both are false.
(e) If assertion is false but reason is true.

1. Assertion : The logic gate NOT can be built using diode.
Reason : The output voltage and the input voltage of the diode have 180° phase difference. **[AIIMS 2005]**

2. Assertion : The number of electrons in a *P*-type silicon semiconductor is less than the number of electrons in a pure silicon semiconductor at room temperature.
Reason : It is due to law of mass action. **[AIIMS 2005]**

3. Assertion : In a common emitter transistor amplifier the input current is much less than the output current.
Reason : The common emitter transistor amplifier has very high input impedance. **[AIIMS 2005]**

4. Assertion : A transistor amplifier in common emitter configuration has a low input impedence.
Reason : The base to emitter region is forward biased. **[AIIMS 2004]**

5. Assertion : The resistivity of a semiconductor increases with temperature.
Reason : The atoms of a semiconductor vibrate with larger amplitude at higher temperature there by increasing it's resistivity. **[AIIMS 2003]**

6. Assertion : If the temperature of a semiconductor is increased then it's resistance decreases.
Reason : The energy gap between conduction band and valence band is very small **[AIIMS 1997]**

7. Assertion : The temperature coefficient of resistance is positive for metals and negative for *P-type* semiconductor.
Reason : The effective charge carriers in metals are negatively charged whereas in *P*-type semiconductor they are positively charged. **[AIIMS 1996]**

8. Assertion : Electron has higher mobility than hole in a semiconductor.
Reason : Mass of electron is less than the mass of hole.

9. Assertion : An *N*-type semiconductor has a large number of electrons but still it is electrically neutral.
Reason : An *N*-type semiconductor is obtained by doping an intrinsic semiconductor with a pentavalent impurity.

10. Assertion : The crystalline solids have a sharp melting point.
Reason : All the bonds between the atoms or molecules of a crystalline solids are equally strong, that they get broken at the same temperature.

11. Assertion : Silicon is preferred over germanium for making semiconductor devices.
Reason : The energy gap for germanium is more than the energy gap of silicon.

12. Assertion : We can measure the potential barrier of a *PN* junction by putting a sensitive voltmeter across its terminals.
Reason : The current through the *PN* junction is not same in forward and reversed bias.

13. Assertion : Semiconductors do not Obey's Ohm's law.
Reason : Current is determined by the rate of flow of charge carriers.