10. If the forward voltage in a semiconductor diode is doubled, the width of the depletion layer will

(a) Become half (b) Become one-fourth

(c) Remain unchanged (d) Become double

11. The *PN* junction diode is used as

[CPMT 1972; AFMC 1997; CBSE PMT 1999; AIIMS 1999; RPMT 2000; MP PMT 04]

(a) An amplifier (b) A rectifier

(c) An oscillator (d) A modulator

12. When a *PN* junction diode is reverse biased

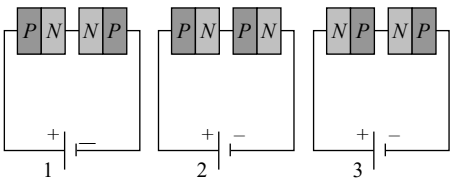
(a) Electrons and holes are attracted towards each other and move towards the depletion region

(b) Electrons and holes move away from the junction depletion region

(c) Height of the potential barrier decreases

(d) No change in the current takes place

13. Two *PN*-junctions can be connected in series by three different methods as shown in the figure. If the potential difference in the junctions is the same, then the correct connections will be **[IIT-JEE 1989]**



(a) In the circuit (1) and (2) (b) In the circuit (2) and (3)

(c) In the circuit (1) and (3) (d) Only in the circuit (1)

14. A *PN*- junction has a thickness of the order of **[BIT 1990]**

(a) $1\,cm$ (b) $1\,mm$

(c) $10^{-6}\,m$ (d) $10^{-12}\,cm$

15. In the depletion region of an unbiased *P-N* junction diode there are **[KCET 1999; CBSE PMT 1999; RPMT 2001; MP PMT 1994, 2003]**

(a) Only electrons

(b) Only holes

(c) Both electrons and holes

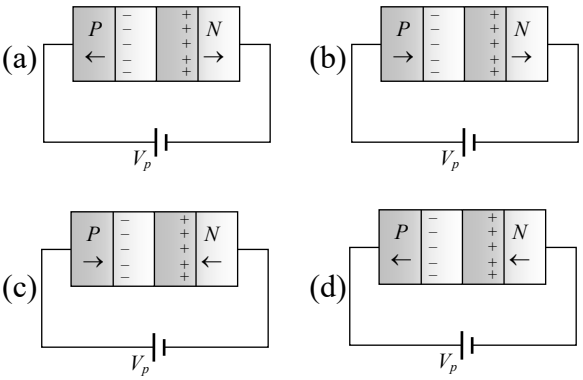
(d) Only fixed ions **[MP PMT 1996]**

16. On increasing the reverse bias to a large value in a *PN*-junction diode, current

(a) Increases slowly (b) Remains fixed

(c) Suddenly increases (d) Decreases slowly

17. In the case of forward biasing of *PN*-junction, which one of the following figures correctly depicts the direction of flow of carriers



18. Which of the following statements concerning the depletion zone of an unbiased *PN* junction is (are) true **[IIT-JEE 1995]**

(a) The width of the zone is independent of the densities of the dopants (impurities)

(b) The width of the zone is dependent on the densities of the dopants

(c) The electric field in the zone is produced by the ionized dopant atoms

(d) The electric field in the zone is provided by the electrons in the conduction band and the holes in the valence band

19. A semiconductor device is connected in a series circuit with a battery and a resistance. A current is found to pass through the circuit. If the polarity of the battery is reversed, the current drops almost to zero. The device may be **[MP PET 1995; CBSE PMT 1998]**

(a) A *P*-type semiconductor (b)

(c) A *PN*-junction (d) An intrinsic semiconductor

20. The approximate ratio of resistances in the

forward and reverse bias of the *PN*-junction diode is

[MP PET 2000; MP PMT 1999, 2002, 03; Pb. PMT 2003]

(a) $10^2 : 1$ (b) $10^{-2} : 1$

(c) $1 : 10^{-4}$ (d) $1 : 10^4$

21. In a junction diode, the holes are due to

[CBSE PMT 1999; Pb. PMT 2003]

(a) Protons (b) Neutrons

(c) Extra electrons (d) Missing of electrons

22. In forward bias, the width of potential barrier in a *P-N* junction diode [EAMCET (Engg.) 1995; CBSE PMT 1999 RPMT 1997, 2002, 03]

(a) Increases

(b) Decreases

(c) Remains constant

(d) First increases then decreases

23. The cause of the potential barrier in a *P-N* diode is

[CBSE PMT 1998; RPMT 2001]

(a) Depletion of positive charges near the junction

(b) Concentration of positive charges near the junction

(c) Depletion of negative charges near the junction

(d) Concentration of positive and negative charges near the junction

24. In a *PN*-junction diode not connected to any circuit

[IIT-JEE 1998]

(a) The potential is the same everywhere

(b) The *P*-type is a higher potential than the *N*-type side

(c) There is an electric field at the junction directed from the *N*- type side to the *P*- type side

(d) There is an electric field at the junction directed from the *P*-type side to the *N*-type side

25. Which of the following statements is not true

[IIT-JEE 1997 Re-Exam]

(a) The resistance of intrinsic semiconductors decrease with increase of temperature

(b) Doping pure *Si* with trivalent impurities give *P*-type semiconductors

(c) The majority carriers in *N*-type semiconductors are holes

(d) A *PN*-junction can act as a semiconductor diode

26. The dominant mechanisms for motion of charge carriers in forward and reverse biased silicon *P-N* junctions are

[IIT-JEE 1997 Cancelled; RPMT 2000; AIIMS 2000]

(a) Drift in forward bias, diffusion in reverse bias

(b) Diffusion in forward bias, drift in reverse bias

(c) Diffusion in both forward and reverse bias

(d) Drift in both forward and reverse bias

27. In *P-N* junction, avalanche current flows in circuit when biasing is [RPET 1997]

(a) Forward (b) Reverse

(c) Zero (d) Excess

28. The depletion layer in the *P-N* junction region is caused by

[CBSE PMT 1994]

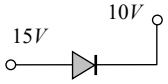
(a) Drift of holes

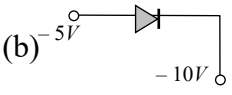
(b) Diffusion of charge carriers

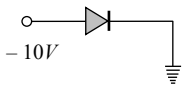
(c) Migration of impurity ions

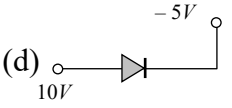
(d) Drift of electrons

29. Which one is reverse-biased

(a) 

(b) 

(c) 

(d) 

30. In a *P-N* junction diode if *P* region is heavily doped than *n* region then the depletion layer is

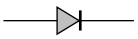
(a) Greater in *P* region

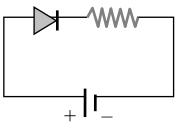
(b) Greater in *N* region

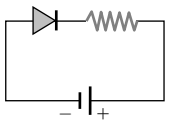
(c) Equal in both region

(d) No depletion layer is formed in this case

31. Which one is in forward bias

(a) 

(b) 

(c) 

(d) None of these

32. The reason of current flow in *P-N* junction in forward bias is **[RPMT 2000]**

(a) Drifting of charge carriers

(b) Minority charge carriers

(c) Diffusion of charge carriers

(d) All of these

33. The resistance of a reverse biased *P-N* junction diode is about **[MP PMT 2000]**

(a) 1 *ohm* (b) 10^2 *ohm*

(c) 10^3 *ohm* (d) 10^6 *ohm*

34. Consider the following statements *A* and *B* and identify the correct choice of the given answers

A: The width of the depletion layer in a *P-N* junction diode increases in forwards bias

B: In an intrinsic semiconductor the fermi energy level is exactly in the middle of the forbidden gap **[EAMCET (Engg.) 2000]**

(a) *A* is true and *B* is false (b) Both *A* and *B* are false

(c) *A* is false and *B* is true (d)Both *A* and *B* are true

35. In comparison to a half wave rectifier, the full wave rectifier gives lower

(a) Efficiency (b) Average *dc*

(c) Average output voltage (d) None of these

36. Avalanche breakdown is due to

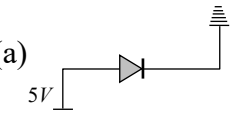
(a) Collision of minority charge carrier

(b) Increase in depletion layer thickness

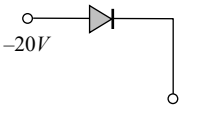
(c) Decrease in depletion layer thickness **[RPMT 1999]**

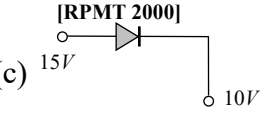
(d) None of these

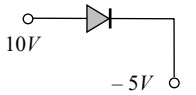
37. Which is reverse biased diode

(a) 

[RPMT 2000]

(b) 

(c) 

(d) 

38. Zener breakdown in a semi-conductor diode occurs when **[UPSEAT 2002]**

(a) Forward current exceeds certain value

(b) Reverse bias exceeds certain value

(c) Forward bias exceeds certain value

(d) Potential barrier is reduced to zero

39. When forward bias is applied to a *P-N* junction, then what happens to the potential barrier V_B, and the width of charge depleted region *x* **Roorkee 1999; RPET 2003; AIEEE 2004]**

(a) V_B increases, *x* decreases

(b) V_B decreases, *x* increases

(c) V_B increases, *x* increases

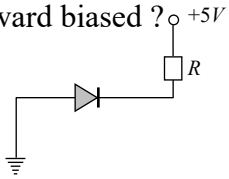
(d) V_B decreases, *x* decreases

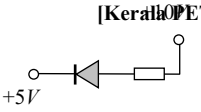
40. The potential barrier, in the depletion layer, is due to **[EAMCET (Engg.) 1998; Pb. PMT 1999; Pb. PET 2001; AIIMS 2002]**

(a) Ions (b) Holes

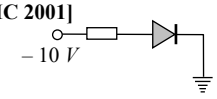
(c) Electrons (d) Both (b) and (c)

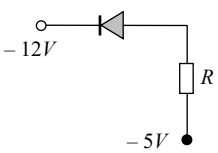
41. In the given figure, which of the diodes are forward biased ? **[Kerala PET 2002]**

1. 

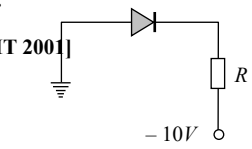
2. 

[AFMC 2001]

3. 

4. 

[RPMT 2001]



5.

(a) 1, 2, 3 (b) 2, 4, 5

(c) 1, 3, 4 (d) 2, 3, 4

42. Function of rectifier is **[AFMC 2002, 04]**

(a) To convert *ac* into *dc* (b) To convert *dc* into *ac*

(c) Both (a) and (b) (d) None of these

43. When the *P* end of *P-N* junction is connected to the negative terminal of the battery and the *N* end to the positive terminal of the battery, then the *P-N* junction behaves like

(a) A conductor (b) An insulator

(c) A super-conductor (d) A semi-conductor

44. If the two ends *P* and *N* of a *P-N* diode junction are joined by a wire **[MP PMT 2002]**

(a) There will not be a steady current in the circuit

(b) There will be a steady current from *N* side to *P* side

(c) There will be a steady current from *P* side to *N* side

(d) There may not be a current depending upon the resistance of the connecting wire

45. A potential barrier of 0.50 *V* exists across a *P-N* junction. If the depletion region is $5.0\times10^{-7}\,m$ wide, the intensity of the electric field in this region is **[UPSEAT 2002]**

(a) $1.0\times10^{6}\ V/m$ (b) $1.0\times10^{5}\ V/m$

(c) $2.0\times10^{5}\ V/m$ (d) $2.0\times10^{6}\ V/m$

46. If no external voltage is applied across *P-N* junction, there would be

(a) No electric field across the junction

(b) An electric field pointing from *N*-type to *P*-type side across the junction

(c) An electric field pointing from *P*-type to *N*-type side across the junction

(d) A temporary electric field during formation of *P-N* junction that would subsequently disappear

47. In a *PN*-junction **[CBSE PMT 2002]**

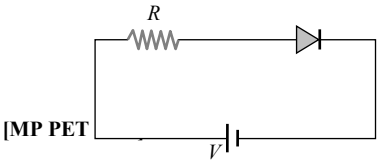
(a) *P* and *N* both are at same potential

(b) High potential at *N* side and low potential at *P* side

(c) High potential at *P* side and low potential at *N* side

(d) Low potential at *N* side and zero potential at *P* side

48. For the given circuit of *PN*-junction diode, which of the following statement is correct



[MP PET

(a) In forward biasing the voltage across *R* is *V*

(b) In forward biasing the voltage across *R* is 2*V*

(c) In reverse biasing the voltage across *R* is *V*

(d) In reverse biasing the voltage across *R* is 2*V*

49. On adjusting the *P-N* junction diode in forward biased

[RPET 2003]

(a) Depletion layer increases (b)

(c) Both decreases (d) None of these

50. In the middle of the depletion layer of a reverse-biased *PN* junction, the

(a) Potential is zero (b) Electric field is zero

(c) Potential is maximum (d) Electric field is maximu

51. Barrier potential of a *P-N* junction diode does not depend on

(a) Temperature (b) Forward bias

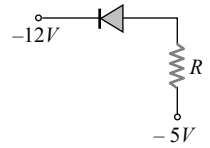
[Orissa JEE 2002] (c) Doping density (d) Diode design

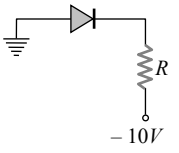
52. A crystal diode is a **[MP PET 2004]**

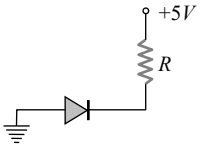
(a) Non-linear device (b) Amplifying device

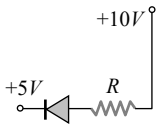
(c) Linear device (d) Fluctuating device

53. Of the diodes shown in the following diagrams, which one is reverse biased

(a) 

(b) 

(c) 

(d) 

54. In a *PN* junction photo cell, the value of photo-electromotive force produced by monochromatic light is proportional to **[CBSE PMT 2004]**

(a) The voltage applied at the *PN* junction

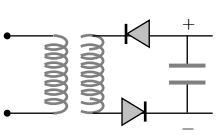
(b) The barrier voltage at the *PN* junction

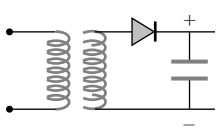
(c) The intensity of the light falling on the cell

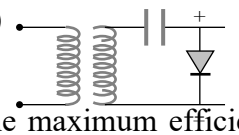
(d) The frequency of the light falling on the cell

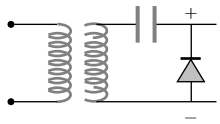
55. Which is the correct diagram of a half-wave rectifier

[Orissa PMT 2004]

(a) 

(b) 

(c) 

(d) 

56. The maximum efficiency of full wave rectifier is

[J & K CET 2004]

(a) 100% (b) 25.20%

(c) 40.2% (d) 81.2%

57. Serious draw back of the semiconductor device is

[Pb. PMT 2004]

(a) They cannot be used with high voltage

(b) They pollute the environment

(c) They are costly

(d) They do not last for long time

58. Select the correct statement

(a) In a full wave rectifier, two diodes work alternately

(b) In a full wave rectifier, two diodes work simultaneously

(c) The efficiency of full wave and half wave rectifiers is same

(d) The full wave rectifier is bi-directional.

59. In order to forward bias a *PN* junction, the negative terminal of battery is connected to

(a) *P*–side (b) Either *P*–side or *N*–side

(c) *N*–side (d) None of these

60. The diode shown in the circuit is a silicon diode. The potential difference between the points *A* and *B* will be

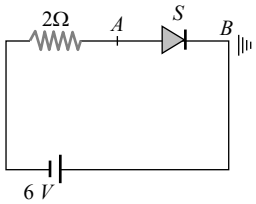
[RPMT 2002]

(a) 6 *V*

(b) 0.6 *V*

(c) 0.7 *V*

(d) 0 *V*



61. Zener breakdown takes place if

(a) Doped impurity is low (b) Doped impurity is high

(c) Less impurity in *N*-part (d)

62. Consider the following statements *A* and *B* and identify the correct choice of the given answers

(A) A zener diode is always connected in reverse bias

(B) The potential barrier of a *PN* junction lies between 0.1 to 0.3 *V* approximately **[EAMCET 2000]**

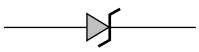
(a) *A* and *B* are correct

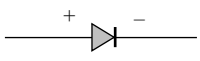
(b) *A* and *B* are wrong

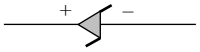
(c) *A* is correct but *B* is wrong

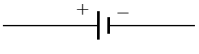
(d) *A* is wrong but *B* is correct

63. The correct symbol for zener diode is **[RPMT 2000]**

(a)  **[RPMT 2003]**

(b) 

(c) 

(d) 

64. Which one of the following statements is not correct

[SCRA 2000]

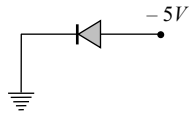
(a) A diode does not obey Ohm's law

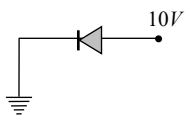
(b) A *PN* junction diode symbol shows an arrow identifying the direction of current (forward) flow

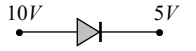
(c) An ideal diode is an open switch

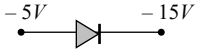
(d) An ideal diode is an ideal one way conductor

65. Which of the following semi-conductor diodes is reverse biased **[DPMT 2000]**

(a) 

(b) 

(c) 

(d) 

66. No bias is applied to a *P-N* junction, then the current **[RPMT 1999]**

(a) Is zero because the number of charge carriers flowing on both sides is same

(b) Is zero because the charge carriers do not move

(c) Is non-zero

(d) None of these

67. Zener diode is used as **[CBSE PMT 1999]**

(a) Half wave rectifier (b) Full wave rectifier

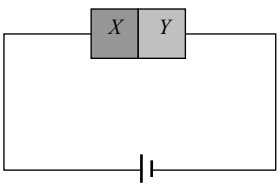
(c) ac voltage stabilizer (d) dc voltage stabilizer

68. The width of forbidden gap in silicon crystal is 1.1 *eV*. When the crystal is converted in to a *N*-type semiconductor the distance of Fermi level from conduction band is **[EAMCET (Med.) 1999]**

(a) Greater than 0.55 *eV* (b) Equal to 0.55 *eV*

(c) Lesser than 0.55 *eV* (d) Equal to 1.1 *eV*

69. A semiconductor *X* is made by doping a germanium crystal with arsenic (Z = 33). A second semiconductor *Y* is made by doping germanium with indium (Z = 49). The two are joined end to end and connected to a battery as shown. Which of the following statements is correct **[Orissa JEE 1998]**



(a) *X* is *P*-type, *Y* is *N*-type and the junction is forward biased

(b) *X* is *N*-type, *Y* is *P*-type and the junction is forward biased

(c) *X* is *P*-type, *Y* is *N*-type and the junction is reverse biased

(d) *X* is *N*-type, *Y* is *P*-type and the junction is reverse biased

70. In *P-N* junction, the barrier potential offers resistance to **[AMU 1995, 96]**

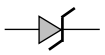
(a) Free electrons in *N* region and holes in *P* region

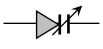
(b) Free electrons in *P* region and holes in *N* region

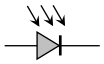
(c) Only free electrons in *N* region

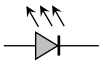
(d) Only holes in *P* region

71. Symbolic representation of photodiode is **[RPMT 1995]**

(a) 

(b) 

(c) 

(d) 

72. To make a *PN* junction conducting **[IIT-JEE 1994]**

(a) The value of forward bias should be more than the barrier potential

(b) The value of forward bias should be less than the barrier potential

(c) The value of reverse bias should be more than the barrier potential

(d) The value of reverse bias should be less than the barrier potential

73. Which is the wrong statement in following sentences? A device in which *P* and *N*-type semiconductors are used is more useful then a vacuum type because **[MP PET 1992]**

(a) Power is not necessary to heat the filament

(b) It is more stable

(c) Very less heat is produced in it

(d) Its efficiency is high due to a high voltage across the junction

74. The depletion layer in silicon diode is 1 μm wide and the knee potential is 0.6 V, then the electric field in the depletion layer will be

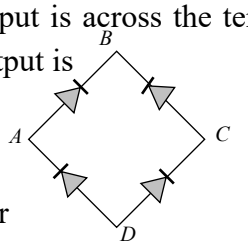
(a) Zero

(b) 0.6 Vm^{-1}

(c) 6×10^4 V/m

(d) 6×10^5 V/m

75. In the diagram, the input is across the terminals A and C and the output is across the terminals B and D, then the output is



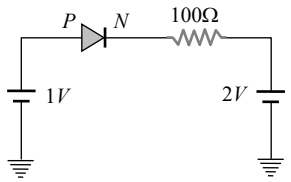
(a) Zero

(b) Same as input

(c) Full wave rectifier

(d) Half wave rectifier

76. The current through an ideal PN-junction shown in the following circuit diagram will be



(a) Zero

(b) 1 mA

(c) 10 mA

(d) 30 mA

77. If a full wave rectifier circuit is operating from 50 Hz mains, the fundamental frequency in the ripple will be

[UPSEAT 2000; CBSE PMT 2003; AIEEE 2005]

(a) 50 Hz (b) 70.7 Hz

(c) 100 Hz (d) 25 Hz

78. In a full wave rectifiers, input ac current has a frequency 'ν'. The output frequency of current is **[BHU 2005]**

(a) $\nu/2$ (b) ν

(c) 2ν (d) None of these

79. A diode having potential difference 0.5 V across its junction which does not depend on current, is connected in series with resistance of 20 Ω across source. If 0.1 A passes through resistance then what is the voltage of the source

[DCE 2005]

(a) 1.5 V (b) 2.0 V

(c) 2.5 V (d) 5 V

Junction Transistor

1. When NPN transistor is used as an amplifier

[AIEEE 2004]

(a) Electrons move from base to collector

(b) Holes move from emitter to base

(c) Electrons move from collector to base **[CBSE PMT 1994]**

(d) Holes move from base to emitter

2. The phase difference between input and output voltages of a CE circuit is

(a) 0^o (b) 90^o

(c) 180^o (d) 270^o

3. An oscillator is nothing but an amplifier with **[AMU 1998]**

[MP PET 2004]

(a) Positive feed back (b) Large gain

(c) No feedback (d) Negative feedback

4. The emitter-base junction of a transistor is …… biased while the collector-base junction is ……. biased

[KCET 2004]

(a) Reverse, forward (b) Reverse, reverse

(c) Forward, forward (d) Forward, reverse

5. In an NPN transistor the collector current is 24 mA. If 80% of electrons reach collector its base current in mA is

[Kerala PMT 2004]

(a) 36 (b) 26

(c) 16 (d) 6

6. A NPN transistor conducts when

(a) Both collector and emitter are positive with respect to the base

(b) Collector is positive and emitter is negative with respect to the base

(c) Collector is positive and emitter is at same potential as the base

(d) Both collector and emitter are negative with respect to the base

7. In the case of constants α and β of a transistor **[CET 2003]**

(a) $\alpha = \beta$ (b) $\beta < 1 \quad \alpha > 1$

(c) $\alpha\beta = 1$ (d) $\beta > 1 \quad \alpha < 1$

8. Which of the following is true **[DPMT 2002]**

(a) Common base transistor is commonly used because current gain is maximum

(b) Common emitter is commonly used because current gain is maximum

(c) Common collector is commonly used because current gain is maximum

(d) Common emitter is the least used transistor

9. If $\alpha = 0.98$ and current through emitter $i_e = 20$ mA, the value of β is **[DPMT 2002]**

(a) 4.9 (b) 49

(c) 96 (d) 9.6

10. For a common base configuration of PNP transistor $\frac{I_C}{I_E} = 0.98$ then maximum current gain in common emitter configuration will be **[CBSE PMT 2002]**

(a) 12 (b) 24

(c) 6 (d) 5

11. In a PNP transistor working as a common-base amplifier, current gain is 0.96 and emitter current is 7.2 mA. The base current is **[AFMC 2002; Pb. PET 2002]**

(a) 0.4 mA (b) 0.2 mA

(c) 0.29 mA (d) 0.35 mA

12. If l_1, l_2, l_3 are the lengths of the emitter, base and collector of a transistor then **[KCET 2002]**

(a) $l_1 = l_2 = l_3$ (b) $l_3 < l_2 > l_1$

(c) $l_3 < l_1 < l_2$ (d) $l_3 > l_1 > l_2$

13. In an NPN transistor circuit, the collector current is 10 mA. If 90% of the electrons emitted reach the collector, the emitter current (i_E) and base current (i_B) are given by **[KCET 2001]**

(a) $i_E = -1\ mA$, $i_B = 9\ mA$

(b) $i_E = 9\ mA$, $i_B = -1\ mA$

(c) $i_E = 1\ mA$, $i_B = 11\ mA$

(d) $i_E = 11\ mA$, $i_B = 1\ mA$

14. In a common emitter transistor, the current gain is 80. What is the change in collector current, when the change in base current is 250 μA **[CBSE PMT 2000]**

(a) $80 \times 250\ \mu A$ (b) $(250 - 80)\ \mu A$

(c) $(250 + 80)\ \mu A$ (d) $250/80\ \mu A$

15. Least doped region in a transistor

(a) Either emitter or collector

(b) Base

(c) Emitter

(d) Collector

16. The transistors provide good power amplification when they are used in **[CBSE PMT 2002]**

(a) Common collector configuration

(b) Common emitter configuration

(c) Common base configuration

(d) None of these

17. The transfer ratio of a transistor is 50. The input resistance of the transistor when used in the common-emitter configuration is 1 $K\Omega$. The peak value for an A.C input voltage of 0.01 V peak is **[CBSE PMT 1998]**

(a) 100 μA (b) 0.01 mA

(c) 0.25 mA (d) 500 μA

18. For a transistor the parameter $\beta = 99$. The value of the parameter α is **[Pb CET 1998]**

(a) 0.9 (b) 0.99

(c) 1 (d) 9

19. A transistor is used in common emitter mode as an amplifier. Then **[IIT-JEE 1998]**

(a) The base-emitter junction is forward biased

(b) The base-emitter junction is reverse biased

(c) The input signal is connected in series with the voltage applied to the base-emitter junction

(d) The input signal is connected in series with the voltage applied to bias the base collector junction

20. In a *PNP* transistor the base is the *N*-region. Its width relative to the *P*-region is

(a) Smaller (b) Larger

(c) Same (d) Not related

21. A common emitter amplifier is designed with *NPN* transistor (α = 0.99). The input impedance is 1 *K*Ω and load is 10 *K*Ω. The voltage gain will be **[CPMT 1996]**

(a) 9.9 (b) 99

(c) 990 (d) 9900

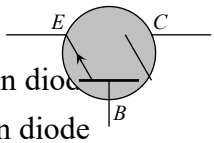
22. The symbol given in figure represents **[AMU 1995, 96]**

(a) *NPN* transistor

(b) *PNP* transistor

(c) Forward biased *PN* junction diode

(d) Reverse biased *NP* junction diode

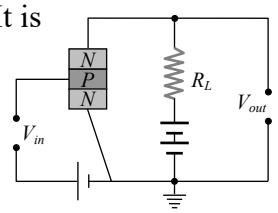


23. The most commonly used material for making transistor is **[MNR 1995]**

(a) Copper (b) Silicon

(c) Ebonite (d) Silver

24. An *NPN*-transistor circuit is arranged as shown in figure. It is **[BHU 1994]**



(a) A common base amplifier circuit

(b) A common emitter amplifier circuit

(c) A common collector amplifier circuit

(d) Neither of the above

25. The part of a transistor which is heavily doped to produce a large number of majority carriers, is **[CBSE PMT 1993]**

(a) Base (b) Emitter

(c) Collector (d) None of these

26. For a transistor, the current amplification factor is 0.8. The transistor is connected in common emitter configuration. The change in the collector current when the base current changes by 6 *mA* is **[DCE 1997] [Haryana CET 1991]**

(a) 6 *mA* (b) 4.8 *mA*

(c) 24 *mA* (d) 8 *mA*

27. In a common base amplifier circuit, calculate the change in base current if that in the emitter current is 2 *mA* and $\alpha = 0.98$ **[BHU 1995]**

(a) 0.04 *mA* (b) 1.96 *mA*

(c) 0.98 *mA* (d) 2 *mA*

28. In case of *NPN*-transistors the collector current is always less than the emitter current because

(a) Collector side is reverse biased and emitter side is forward biased

(b) After electrons are lost in the base and only remaining ones reach the collector

(c) Collector side is forward biased and emitter side is reverse biased

(d) Collector being reverse biased attracts less electrons

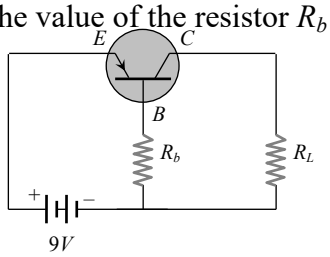
29. In a transistor circuit shown here the base current is 35 μA. The value of the resistor R_b is

(a) 123.5 *k*Ω

(b) 257 *k*Ω

(c) 380.05 *k*Ω

(d) None of these



30. In a transistor, a change of 8.0 *mA* in the emitter current produces a change of 7.8 *mA* in the collector current. What change in the base

current is necessary to produce the same change in the collector current

(a) 50 μA (b) 100 μA

(c) 150 μA (d) 200 μA

31. In a transistor configuration β-parameter is **[Orissa PMT 2004]**

(a) $\frac{I_b}{I_c}$ (b) $\frac{I_c}{I_b}$

(c) $\frac{I_c}{I_a}$ (d) $\frac{I_a}{I_c}$

32. Which of these is unipolar transistor **[Pb PMT 2004]**

(a) Point contact transistor (b) Field effect transistor

(c) *PNP* transistor (d) None of these

33. For a transistor, in a common emitter arrangement, the alternating current gain β is given by **[DPMT 2004]**

(a) $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_C}$ (b) $\beta = \left(\frac{\Delta I_B}{\Delta I_C}\right)_{V_C}$

(c) $\beta = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_C}$ (d) $\beta = \left(\frac{\Delta I_E}{\Delta I_C}\right)_{V_C}$

34. The relation between α and β parameters of current gains for a transistors is given by

(a) $\alpha = \frac{\beta}{1-\beta}$ (b) $\alpha = \frac{\beta}{1+\beta}$

(c) $\alpha = \frac{1-\beta}{\beta}$ (d) $\alpha = \frac{1+\beta}{\beta}$

35. When *NPN* transistor is used as an amplifier **[DCE 2002]**

(a) Electrons move from base to emitter

(b) Electrons move from emitter to base

(c) Electrons moves from base to emitter

(d) Holes moves from base to emitter

36. In the *CB* mode of a transistor, when the collector voltage is changed by 0.5 *volt*. The collector current changes by 0.05 *mA*. The output resistance will be **[Pb. PMT 2003]**

(a) 10 $k\Omega$ (b) 20 $k\Omega$

(c) 5 $k\Omega$ (d) 2.5 $k\Omega$

37. Which of the following is used to produce radio waves of constant amplitude

(a) Oscillator (b) FET

(c) Rectifier (d) Amplifier

38. While a collector to emitter voltage is constant in a transistor, the collector current changes by 8.2 *mA* when the emitter current changes by 8.3 *mA*. The value of forward current ratio h_{fe} is **[KCET 2002]**

(a) 82 (b) 83

(c) 8.2 (d) 8.3

39. Consider an *NPN* transistor amplifier in common-emitter configuration. The current gain of the transistor is 100. If the collector current changes by 1 *mA,* what will be the change in emitter current

(a) 1.1 *mA* (b) 1.01 *mA*

(c) 0.01 *mA* (d) 10 *mA*

40. In a common base amplifier the phase difference between the input signal voltage and the output voltage is **[CBSE PMT 1990; AIEEE 2005]**

(a) 0 (b) $\pi/4$

(c) $\pi/2$ **[Pb. PET 2000]** (d) π

41. In *NPN* transistor the collector current is 10 *mA*. If 90% of electrons emitted reach the collector, then **[Kerala PMT 2005]**

(a) Emitter current will be 9 *mA*

(b) Emitter current will be 11.1 *mA*

(c) Base current will be 0.1 *mA*

(d) Base current will be 0.01 *mA*

42. *NPN* transistor are preferred to *PNP* transistor because they have **[J & K CET 2005]**

(a) Low cost

(b) Low dissipation energy

(c) Capability of handing large power

(d) Electrons having high mobility than holes

43. In a transistor in CE configuration, the ratio of power gain to voltage gain is **[J & K CET 2005]**

(a) α (b) β/α

(c) $\beta\alpha$ (d) β

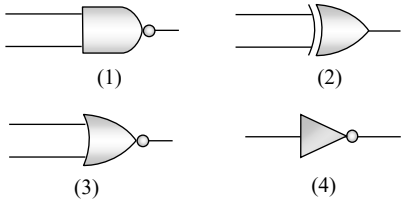
44. In the study of transistor as an amplifier, if $\alpha = I_c / I_e$ and $\beta = I_c / I_b$, where I_c, I_b and I_e are the collector, base and emitter currents, then **[CBSE PMT 2000; KCET 2000; Orissa JEE 2005]**

(a) $\beta = \frac{1-\alpha}{\alpha}$ (b) $\beta = \frac{\alpha}{1-\alpha}$

(c) $\beta = \frac{\alpha}{1+\alpha}$ (d) $\beta = \frac{1+\alpha}{\alpha}$

Digital Electronics

1. Given below are symbols for some logic gates

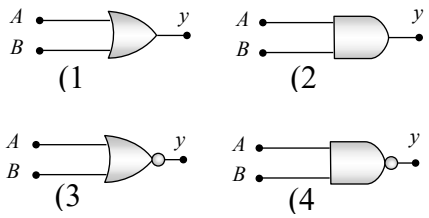


The XOR gate and NOR gate respectively are **[AFMC 1994]**

(a) 1 and 2 (b) 2 and 3

(c) 3 and 4 (d) 1 and 4

2. Given below are four logic gate symbol (figure). Those for OR, NOR and NAND are respectively **[NSEP 1994]**



(a) 1, 4, 3 (b) 4, 1, 2

(c) 1, 3, 4 (d) 4, 2, 1

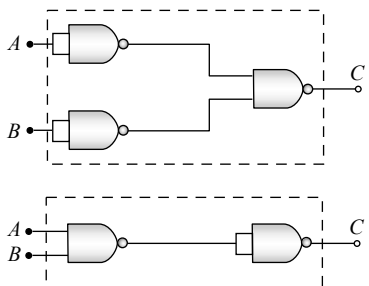
3. The following truth table corresponds to the logic gate **[BHU 1994; CPMT 2000; J & K CET 2004]**

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

(a) NAND (b) OR

(c) AND (d) XOR

4. The combination of 'NAND' gates shown here under (figure) are equivalent to



(a) An OR gate and an AND gate respectively

(b) An AND gate and a NOT gate respectively

(c) An AND gate and an OR gate respectively

(d) An OR gate and a NOT gate respectively.

5. A truth table is given below. Which of the following has this type of truth table **[CBSE PMT 1996; UPS**

A	0	1	0	1
B	0	0	1	1
y	1	0	0	0

(a) XOR gate (b) NOR gate

(c) AND gate (d) OR gate

6. The truth table shown in figure is for **[Pb. CET 1998]**

A	0	0	1	1
B	0	1	0	1
Y	1	0	0	1

(a) XOR (b) AND

(c) XNOR (d) OR

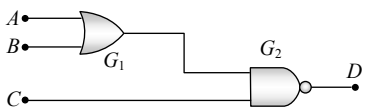
7. For the given combination of gates, if the logic states of inputs A, B, C are as follows $A = B = C = 0$ and $A = B = 1$, $C = 0$ then the logic states of output D are

(a) 0, 0

(b) 0, 1

(c) 1, 0

(d) 1, 1



8. Boolean algebra is essentially based on **[AIIMS 1999]**

(a) Truth (b) Logic

(c) Symbol (d) Numbers

9. The logic behind 'NOR' gate is that it gives **[CPMT 1999, AFMC 1999]**

[Haryana CEET 1996]

(a) High output when both the inputs are low

(b) Low output when both the inputs are low

(c) High output when both the inputs are high

(d) None of these

10. A logic gate is an electronic circuit which **[BHU 2000]**

(a) Makes logic decisions

(b) Allows electrons flow only in one direction

(c) Works binary algebra

(d) Alternates between 0 and 1 values

11. A gate has the following truth table **[CBSE PMT 2000]**

P	1	1	0	0
Q	1	0	1	0
R	1	0	0	0

The gate is

(a) NOR (b) OR

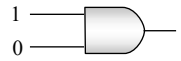
(c) NAND (d) AND

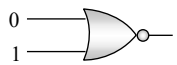
12. How many NAND gates are used to form an AND gate **[MP PET 2004]**

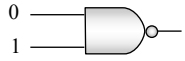
(a) 1 (b) 2

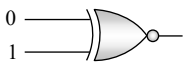
(c) 3 (d) 4

13. Which of the following gates will have an output of 1 **[CBSE PMT 1998]**

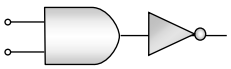
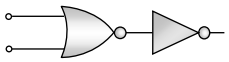
(a) 

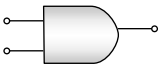
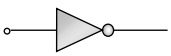
(b) 

(c) 

(d) 

14. Which represents NAND gate

(a)  (b) 

(c)  (d) 

15. The given truth table is of

A	X
0	1
1	0

(a) OR gate (b) AND gate

(c) NOT gate (d) None of above

16. What will be the input of A and B for the Boolean expression $\overline{(A+B)}\cdot\overline{(A\cdot B)}=1$ **[TNPCEE 2002]**

(a) 0, 0 (b) 0, 1

(c) 1, 0 (d) 1, 1

17. If A and B are two inputs in AND gate, then AND gate has an output of 1 when the values of A and B are **[TNPCEE 2002]**

(a) $A = 0, B = 0$ (b) $A = 1, B = 1$

(c) $A = 1, B = 0$ (d) $A = 0, B = 1$

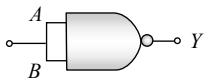
18. The Boolean equation of NOR gate is **[Haryana CET 2002]**

(a) $C = A + B$ (b) $C = \overline{A+B}$

(c) $C = A\cdot B$ (d) $C = \overline{A\cdot B}$

19. This symbol represents **[CBSE PMT 1996]**

(a) NOT gate

(b) OR gate 

(c) AND gate

(d) NOR gate

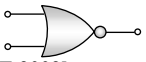
20. Which logic gate is represented by following diagram **[DCE 2001]**

(a) AND

(b) OR 

(c) NOR

(d) XOR

21. Symbol  represents **[Kerala PMT 2001]** **[DCE 2002]**

(a) NAND gate (b) NOR gate

(c) NOT gate (d) XNOR gate

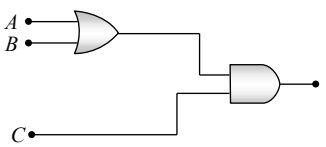
22. To get an output 1 from the circuit shown in the figure, the input must be **[AMU 1998; J & K CET 2002]**

(a) $A = 0, B = 1, C = 0$

(b) $A = 1, B = 0, C = 0$

(c) $A = 1, B = 0, C = 1$

(d) $A = 1, B = 1, C = 0$

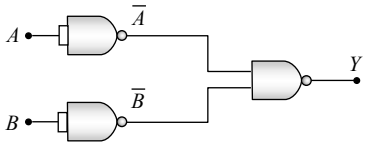


23. The combination of the gates shown in the figure below produces **[DCE 2002]**

(a) NOR gate

(b) OR gate

(c) AND gate



(d) XOR gate

24. The output of a NAND gate is 0

(a) If both inputs are 0

(b) If one input is 0 and the other input is 1

(c) If both inputs are 1

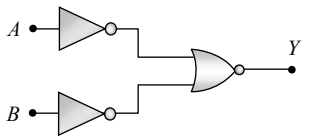
(d) Either if both inputs are 1 or if one of the inputs is 1 and the other 0

25. A gate in which all the inputs must be low to get a high output is called

(a) A NAND gate (b) An inverter

(c) A NOR gate (d) An AND gate

26. Which logic gate is represented by the following combination of logic gates



(a) OR (b) NAND

(c) AND (d) NOR

27. The output of OR gate is 1

(a) If both inputs are zero

(b) If either or both inputs are 1

(c) Only if both input are 1

(d) If either input is zero

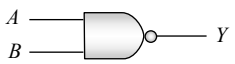
28. Which gates is represented by this figure **[DCE 2003]**

(a) NAND gate

(b) AND gate

(c) NOT gate

(d) OR gate



29. Sum of the two binary numbers $(1000010)_2$ and $(11011)_2$ is

(a) $(111101)_2$ (b) $(111111)_2$

(c) $(101111)_2$ (d) $(111001)_2$

30. The truth-table given below is for which gate **[CBSE PMT 1994, 98 2002; DPMT 2002; BCECE 2005]**

A	0	0	1	1
B	0	1	0	1
C	1	1	1	0

(a) XOR (b) OR

[UPSEAT 2004] (c) AND (d) NAND

31. Which of the following logic gate is an universal gate **[AIIMS 2005]**

(a) OR (b) NOT

(c) AND (d) NOR

Valve Electronics (Diode and Triode)

[UPSEAT 2004]

1. Thermionic emission from a heated filament varies with its temperature T as **[CBSE PMT 1990; RPMT 2000; CPMT 2002]**

(a) T^{-1} (b) T

(c) T^2 **[AIIMS 2004]** (d) $T^{3/2}$

2. Number of secondary electrons emitted per number of primary electrons depends on

(a) Material of target

(b) Frequency of primary electrons

(c) Intensity

(d) None of the above

3. Due to S.C.R in vacuum tube **[CBSE PMT 2004]**

(a) $I_p \rightarrow$ Decrease (b) $I_p -$ Increase

(c) $V_p =$ Increase (d) $V_g =$ Increase

4. In diode, when there is saturation current, the plate resistance (r_p) is **[AIIMS 1997; Haryana PMT 2000]**

(a) Zero (b) Infinite

(c) Some finite quantity (d) Data is insufficient

5. The grid voltage of any triode valve is changed from –1 volt to – 3 *volt* and the mutual conductance is 3×10^{-4} *mho*. The change in plate circuit current will be **[MNR 1999]**

[DCE 2004] (a) 0.8 *mA* (b) 0.6 *mA*

(c) 0.4 *mA* (d) 1 *mA*

6. In a triode, $g_m = 2\times10^{-3}\,ohm^{-1}; \mu = 42$, resistance load, $R = 50$ kilo ohm. The voltage amplification obtained from this triode will be

(a) 30.42 (b) 29.57

(c) 28.18 (d) 27.15

7. In an amplifier the load resistance R_L is equal to the plate resistance (r_p). The voltage amplification is equal to

[CPMT 1995]

(a) μ (b) 2μ

(c) $\mu/2$ (d) $\mu/4$

8. For a given plate-voltage, the plate current in a triode is maximum when the potential of

[IIT-JEE 1985; CPMT 1995; AFMC 1999]

(a) The grid is positive and plate is negative

(b) The grid is positive and plate is positive

(c) The grid is zero and plate is positive

(d) The grid is negative and plate is positive